Module 1

Power Semiconductor Devices

Lesson 3

Power Bipolar Junction Transistor (BJT)

Constructional Features, Operating Principles, Characteristics and specifications of Power Bipolar Junction transistors.

Objective: On completion the student will be able to

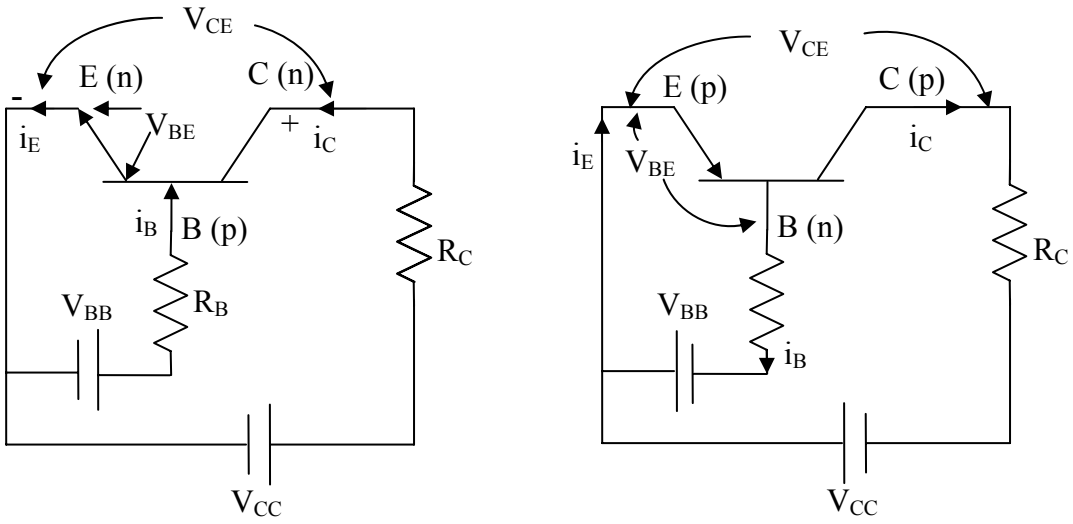
1. Distinguish between, cut off, active, and saturation region operation of a Bipolar Junction Transistor.
2. Draw the input and output characteristics of a junction transistor and explain their nature.
3. List the salient constructional features of a power BJT and explain their importance.
4. Draw the output characteristics of a Power BJT and explain the applicable operating limits under Forward and Reverse bias conditions.
5. Interpret manufacturer's data sheet ratings for a Power BJT.
6. Differentiate between the characteristics of an ideal switch and a BJT.
7. Draw and explain the Turn On characteristics of a BJT.
8. Draw and explain the Turn Off characteristics of a BJT.
9. Calculate switching and conduction losses of a Power BJT.
10. Design a BJT base drive circuit.

3.1 Introduction

Power Bipolar Junction Transistor (BJT) is the first semiconductor device to allow full control over its Turn on and Turn off operations. It simplified the design of a large number of Power Electronic circuits that used forced commutated thyristors at that time and also helped realize a number of new circuits. Subsequently, many other devices that can broadly be classified as "Transistors" have been developed. Many of them have superior performance compared to the BJT in some respects. They have, by now, almost completely replaced BJTs. However, it should be emphasized that the BJT was the first semiconductor device to closely approximate an ideal fully controlled Power switch. Other "transistors" have characteristics that are qualitatively similar to those of the BJT (although the physics of operation may differ). Hence, it will be worthwhile studying the characteristics and operation a BJT in some depth. From the point of view of construction and operation BJT is a bipolar (i.e. minority carrier) current controlled device. It has been used at signal level power for a long time. However, the construction and operating characteristics of a Power BJT differs significantly from its signal level counterpart due to the requirement for a large blocking voltage in the "OFF" state and a high current carrying capacity in the "ON" state. In this module, the construction, operating principle and characteristics of a Power BJT will be explored.

3.2 Basic Operating Principle of a Bipolar Junction Transistor

A junction transistor consists of a semiconductor crystal in which a **p** type region is sandwiched between two **n** type regions. This is called an **n-p-n** transistor. Alternatively an **n** type region may be placed in between two **p** type regions to give a **p-n-p** transistor. Fig 3.1 shows the circuit symbols and schematic representations of an **n-p-n** and a **p-n-p** transistor. The terminals of a transistor are called Emitter (E), Base (B) & Collector (C) as shown in the figure.



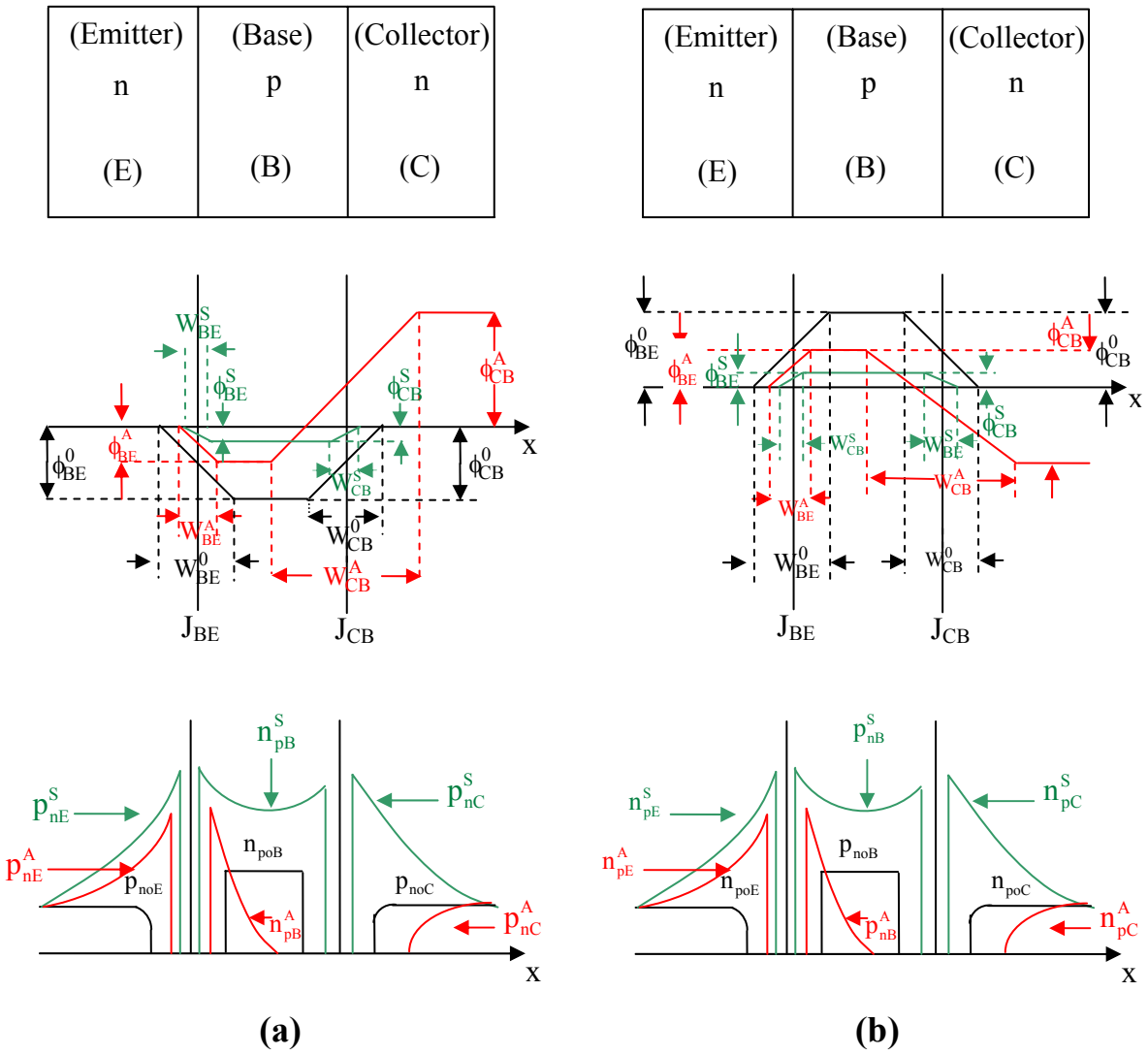


Fig. 3.1: Bipolar junction transistor under different biasing condition.
(a) n – p – n transistor ; (b) p – n – p transistor.

If no external biasing voltages are applied (i.e.; V_{BB} and V_{CC} are open circuited) all transistor currents must be zero. The transistor will be in thermal equilibrium condition with potential barriers ϕ^{o}_{BE} and ϕ^{o}_{CB} at the base emitter and the base collector functions respectively. Corresponding depletion layer widths will be W^{O}_{BE} and W^{O}_{CB}. It is clear from the diagram that **p** type carriers in the base region of an **n-p-n** transistor are trapped in a "potential well" and cannot escape. Similarly, in a **p-n-p** transistor **p** type carriers in the emitter and collector regions are separated by a "potential hill".

When biasing voltages are applied as shown in the figure, the base emitter junction (J_{BE}) becomes forward biased where as the base collector junction is reverse biased. Potential barrier and depletion layer width at J_{BE} reduces to ϕ^{A}_{BE} and W^{A}_{BE} respectively. Both these quantities increase at J_{CB} $\left(\phi^{A}_{CB}, W^{A}_{CB}\right)$. As the potential barrier at J_{BE} is reduced a large number of minority carriers are introduced in to Base and the Emitter regions as shown in Fig. 3.1 (P^{A}_{nE}, n^{A}_{pB} for **n-p-n**

transistor and n_{pE}^{A}, p_{nB}^{A} for **p-n-p** transistor). A portion of the minority carriers reaching the base recombines with majority carriers. The rest, defuse to the edge of the depletion region at J_{CB} where they are swept away to the collector region by the large electric field. Under this condition the transistor is said to be in the Active region.

As V_{BE} is increased injected minority charge into the base region increases and so does the base current and the collector current. For a fixed collector bias voltage V_{CC}, the voltage V_{CB} reduces with increase in collector current due to increasing drop in the external resistance R_C. Therefore, the potential barrier at J_{CB} starts reducing. At one point J_{CB} becomes forward biased. The potential barriers and depletion layer widths under this condition are indicated in Fig. 3.1 by variables with a super script "s". Due to forward biasing of J_{CB} there will be minority carrier injection into the base from this junction also as shown in Fig. 3.1. The total voltage drop between collector and emitter will be the difference between the forward bias voltage drops at J_{BE} and J_{CB}. Under this condition the transistor is said to be in the saturation region.

From the operating principle described above one can form a qualitative idea about the input (i_B vs V_{BE}) and output (i_C Vs V_{CE}) characteristics of a transistor. In the following section these characteristics of an **n-p-n** transistor will be discussed qualitatively. Similar explanation applies to a p-n-p transistor.

When a biasing voltage V_{BB} of appropriate polarity is applied across the junction J_{BE} the potential barrier at this junction reduces and at one point the junction becomes forward biased. The current crossing this junction is governed by the **forward biased p-n junction equation** for a given collector emitter voltage. The base current i_B is related to the recombination of minority carriers injected into the base from the emitter. The rate of recombination is directly proportional to the amount of excess minority carrier stored in the base. Since, in a normal transistor the emitter is much more heavily doped compared to the base the current crossing J_{BE} is almost entirely determined by the excess minority carrier distribution in the base. Thus, it can be concluded that the relationship between i_B and V_{BE} will be similar to the i-v characteristics of a **p-n** junction diode. V_{CE}, however have some effect on this characteristic. As V_{CE} increases reverse bias of J_{CB} increases and the depletion region at J_{CB} moves deeper into the base. The effective base width thus reduces, reducing the rate of recombination in the base region and hence the base current. Therefore i_B for a given V_{BE} reduces with increasing V_{CE} as shown in Fig. 3.2(a).

It has been mentioned before that only a fraction (denoted by the letter "$\propto$") of the total minority carriers injected into the base reaches junction J_{CB} where they are swept in to the collector region by the large electric field at J_{CB}. These minority carriers constitute the major component of the total collector current. The other component of the collector current consists of the small reverse saturation current of the reverse biased junction J_{CB}.

Therefore $$I_C = \propto I_E + I_{cs} \quad (3.1)$$

Where I_{cs} is the reverse saturation current of junction J_{CB}

But $$I_E = I_B + I_C \quad (3.2)$$

$$\therefore I_C = \frac{I_{CS}}{1-\alpha} + \frac{\alpha}{1-\alpha} I_B \qquad (3.3)$$

By defining $\beta \triangleq \frac{\alpha}{1-\alpha}$

$$I_C = \beta I_B + (\beta+1) I_{cs} \qquad (3.4)$$

β is called the large signal common emitter current gain of the transistor and remains fairly constant for a large range of I_C, as shown in Fig. 3.2 (c). Fig: 3 (b) shows the complete out put characteristics (i_c vs V_{CE}) of an n-p-n transistor.

With $V_{BB} = 0$ or negative there is little injected minority carrier into the base from the emitter side. Therefore, $i_B = 0$ and i_C is negligibly small. The transistor is said to be in the "cut off" region under this condition.

As V_{BB} is increased from zero, base current starts flowing. From equation (3.4) it will be expected that the collector current should increase proportionately independent of V_{CE}. However Fig 3.2 (b) does indicate a slight increase in i_C with V_{CE} for a given i_B. This is expected because with increasing V_{CE} a larger value of V_{BE} will be required to maintain a given i_B (Fig. 3.2 (a)). Therefore, the component "αI_E" of collector current will increase. I_{CS} is ,for all practical purpose, independent of V_{CE}. This is the active or "amplifier mode" of operation of a transistor.

In the active region as i_B increases i_C also increases. For a given value of V_{CC}, V_{CE} reduces with increasing i_C due to increased drop in an external load (i.e., Rc in Fig 3.1). At one point the junction J_{CB} becomes forward biased. V_{CE}, now is just the difference between the voltages across two forward biased junction J_{BE} and J_{CB} (a few handed milli volts). This is when the transistor enters the saturation mode of operation. The ratio i_C/i_B at the onset of saturation is called β_{Min} and is an important parameter for a power transistor. In saturation i_C is almost entirely determined by the external load and further increase in i_B changes i_C or V_{CE} very little.

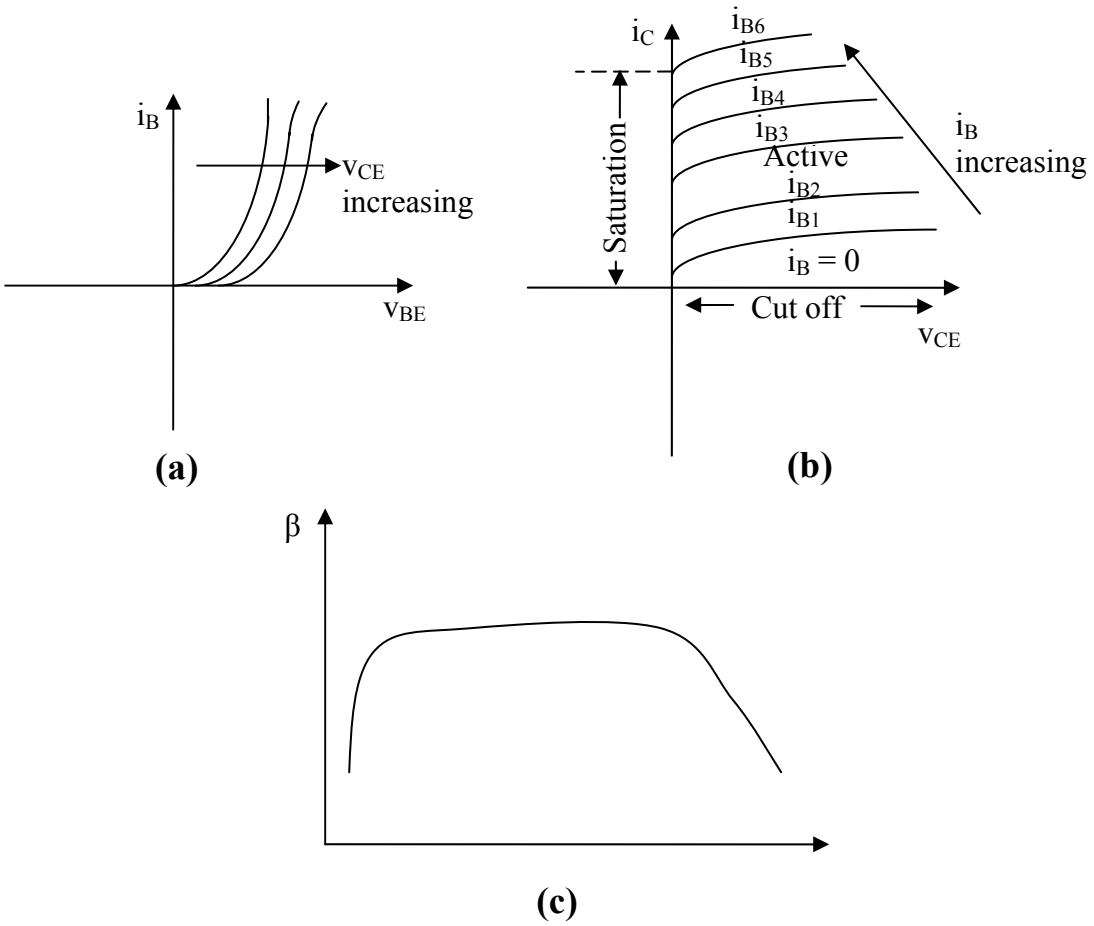


Fig. 3.2: Input and output characteristics of an n – p – n transistor. (a) Input characteristics; (b) Output characteristics; (c) Current gain[β] characteristics

Exercise 3.1

Fill in the blank(s) with the appropriate word(s)

a) Under forward bias condition a large number of _____ carriers are introduced in the base region.

b) Some minority charge carriers reaching base _____ with majority carriers there and the rest of them _____ to the collector.

c) When the base-emitter junction of a BJT is forward biased while the base-collector junction is reverse biased the BJT is said to be in the _____ region.

d) When both B-E & C-B junction of a BJT are reverse biased it is said to be in the _____ region.

e) When both B-E & C-B junction of a BJT are forward biased it is said to be in the _____ region.

Answer: (a) minority; (b) recombine, diffuse; (c) active; (d) cut-off; (e) saturation.

Exercise 3.2

Why does the collector current of a BJT in the active region increases with increasing collector voltage for a given base current.

Answer: In the active region as the V_{CE} voltage is increased the depletion layer width at the CB junction increases and the effective base width reduces. Therefore, for a given V_{BE} recombination of minority carriers in the base region reduces and base current also reduces. In order to main constant base current with increasing V_{CE}, V_{BE} must increased. Therefore, for a constant base current the number of minority carriers in the base region will increase and consequently, collector current will increase.

Exercise 3.3

A power BJT has $I_C = 20$ A at $I_B = 2.5$ A. $I_{cs} = 15$ mA. Find out β & $\propto$.

Answer: $I_c = \beta I_B + (\beta + 1) I_{cs} = \beta(I_B + I_{cs}) + I_{cs}$.

$\therefore \beta = 7.95$,

3.3 Constructional Features of a Power BJT

Power transistors face the same conflicting design requirements (i.e. large off state blocking voltage and large on state current density) as that of a power diode. Therefore, it is only natural to extend some of the constructional features of power diodes to power BJT. Following Section summarizes some of the constructional features of a Power BJT. Since Power Transistors are predominantly of the n-p-n type, in this section and subsequently only this type of transistor will be discussed.

- A power BJT has a vertically oriented alternating layers of **n** type and **p** type semiconductor materials as shown in Fig 3.3(a). The vertical structure is preferred for power transistors because it maximizes the cross sectional area through which the on state current flows. Thus, on state resistance and power lass is minimized.

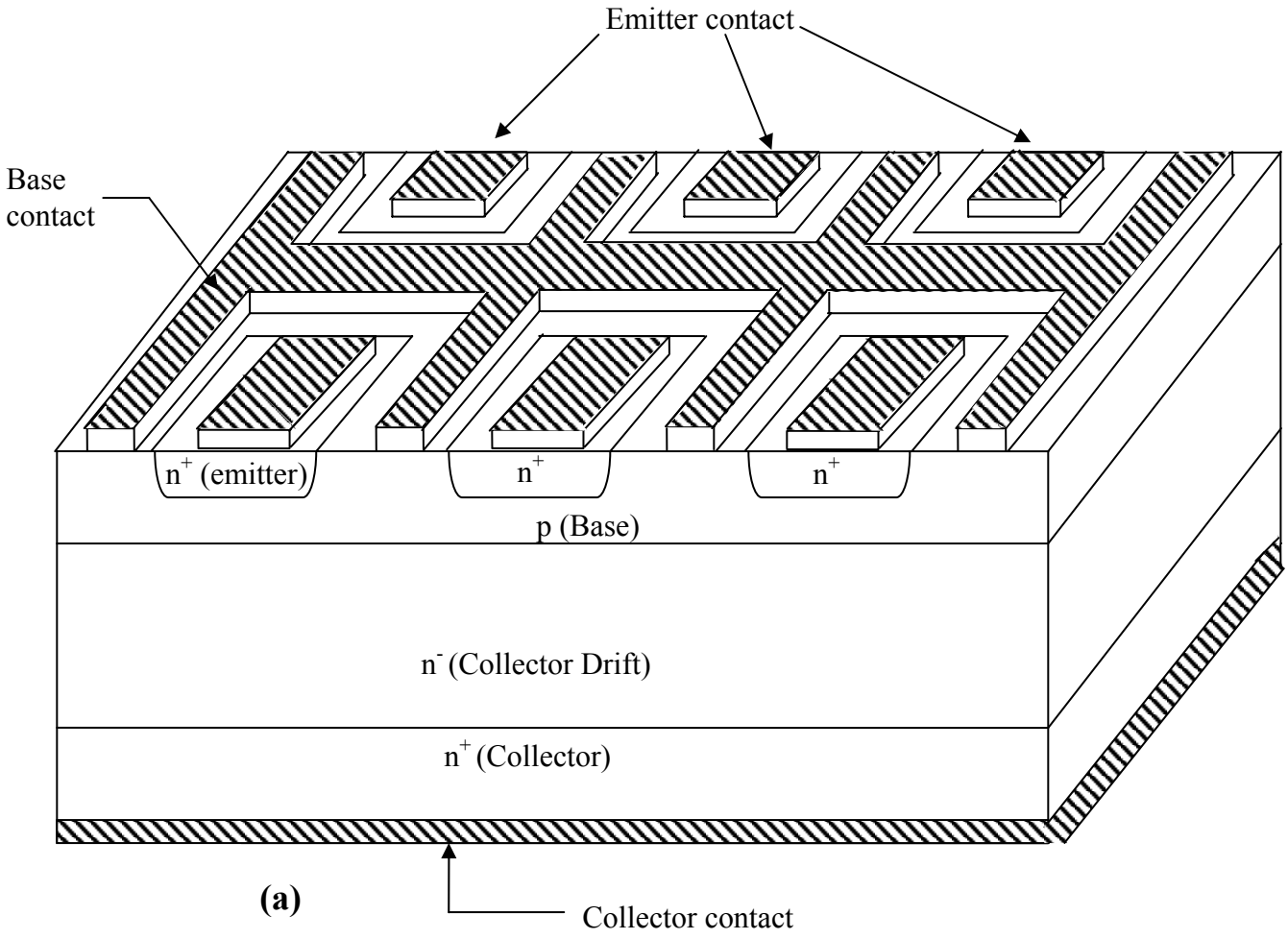
- In order to maintain a **large current gain "β"** (and hence reduce base drive current) the emitter doping density is made several orders of magnitude higher than the base region. The thickness of the base region is also made as small as possible.

- In order to block large voltage during "OFF" state a lightly doped "collector drift region" is introduced between the moderately doped base region and the heavily doped collector region. The function of this **drift region** is similar to that in a Power Diode. However, the doping density donation of the base region being "moderate" the depletion region does penetrate considerably into the base. Therefore, the width of the base region in a power transistor can not be made as small as that in a signal level transistor. This comparatively larger base width has adverse effect on the current gain (β) of a Power transistor which

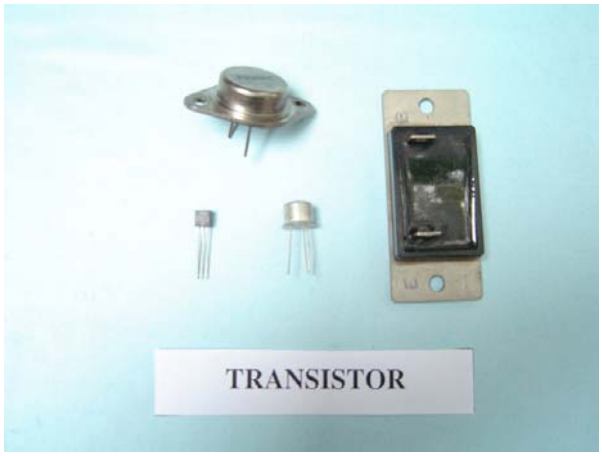
typically varies within 5-20. As will be discusses later the collector drift region has significant effect on the out put characteristics of a Power BJT.

- Practical Power transistors have their emitters and bases interleaved as narrow fingers. This is necessary to prevent **"current crowding"** and consequent **"second break down"**. In addition multiple emitter structure also reduces parasitic ohmic resistance in the base current path.

These constructional features of a Power BJT are shown schematically in Fig 3.3(a). Fig.3.3 (b) shows the photograph of some community available Power transistors in different packages.



(a)



(b)

Fig. 3.3: Constructional Features of a Power Bipolar Junction Transistor
(a) Schematic of Construction,
(b) Photograph of commercial packages.

Exercise 3.4

Fill in the blank(s) with the appropriate word(s)

a) Doping density of the emitter of a Power BJT is several orders of magnitude _____ than the base doping density.
b) Collector drift region is introduced in a Power BJT to block _____ voltage.
c) Doping density of the base region in a power BJT is _____.
d) Power BJT has _____ DC current gain compared to signal level transistors.
e) In a Power BJT multiple, narrow finger like distributed emitter structure is used to avoid emitter _____.

Answer: (a) higher; (b) high reverse; (c) moderate; (d) low; (e) current crowding.

Exercise 3.5

What are the constructional features of a power transistor that affect the dc current gain?

- Large doping density of the emitter increases dc current gain.
- Moderately doped base regain of relatively larger width tend to reduce the dc current gain. The base width in a power transistor cannot be reduced below a certain level in order to avoid "reach through" of the base region under large applied voltage.
- Multiple, narrow emitter regions distributed uniformly over the entire device cross section also tends to improve dc current gain by minimizing "current crowding".

3.4 Output i-v characteristics of a Power Transistor

A typical output (i_C vs V_{CE}) characteristics of an **n-p-n** type power transistor is shown in Fig 3.4 A power transistor exhibits "Cut off", "Active" and "Saturation regions" of operation in its output characteristics similar to a signal level transistor. In fact output characteristics of a

Power Transistor in the "Cut off" and "Active" regions are qualitatively identical to a signal level transistor. Certain quantitative restrictions apply, however, which are discussed next.

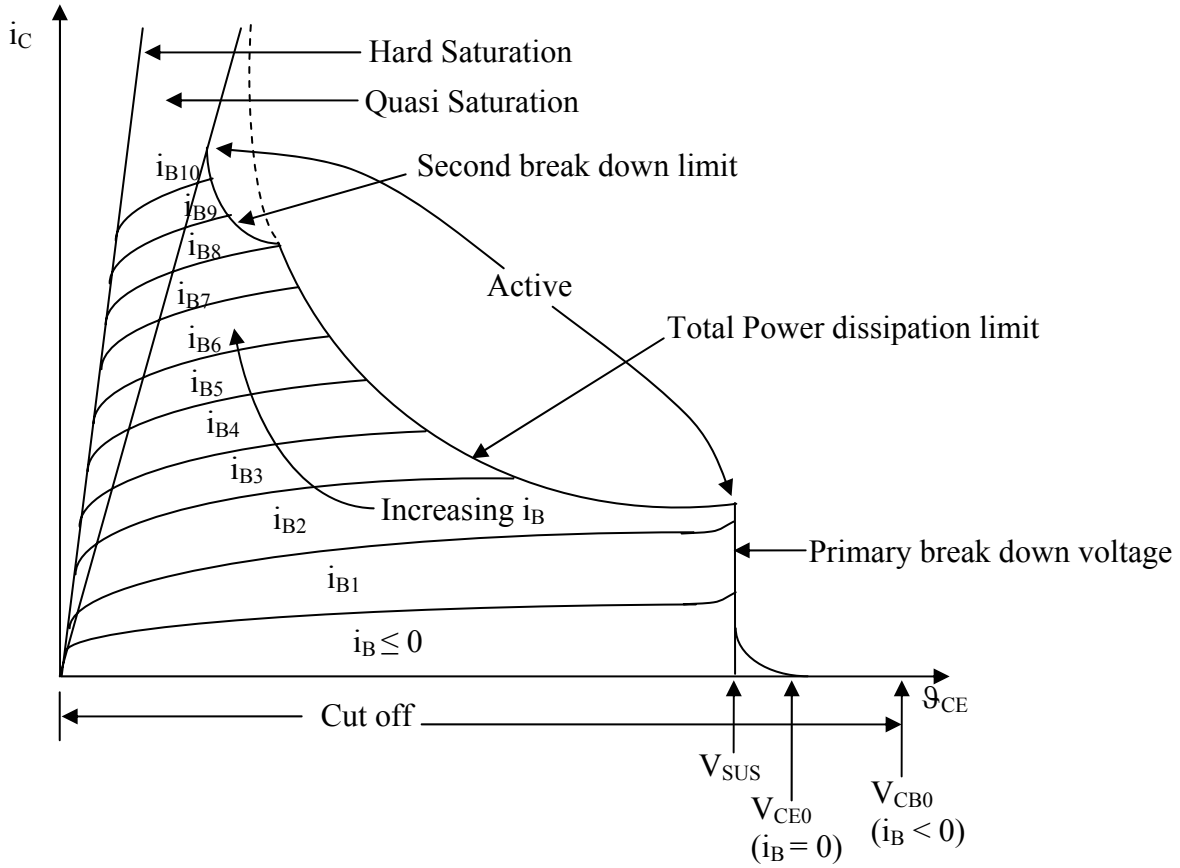


Fig. 3.4 Output ($i_c - v_{CE}$) characteristics of an n – p – n type Power Transistor

In the cut off region ($i_B \leq 0$) the collector current is almost zero. The maximum voltage between collector and emitter under this condition is termed "Maximum forward blocking voltage with base terminal open ($i_B = 0$)" and is denoted by V_{CEO}. For all practical purpose this is the maximum voltage that can be applied in the forward direction (C positive with respect to E) across a power transistor since a power transistor is expected to see any significant forward voltage only with $i_B = 0$. This blocking voltage can however be increased to a value V_{CBO} by keeping the emitter terminal open. In this case $i_B < o$. Actually V_{CBO} is the breakdown voltage of the collector base junction. However, since the open base configuration is more common the value of V_{CEO} is used by the manufacturers as the maximum voltage rating of a power transistor. Power transistors have poor reverse voltage withstanding capability due to low break down voltage of the base-emitter junction. Therefore, reverse voltage (C negative with respect to E) should not appear across a power transistor.

In the active region the ratio of collector current to base current (DC current Gain (β)) remains fairly constant upto certain value of the collector current after which it falls off rapidly. Manufacturers usually provide a graph showing the variation of β as a function of the collector current for different junction temperatures and collector emitter voltages. This graph is useful for designing the base drive of a Power transistor. Typically, the value of the dc current gain of a Power transistor is much smaller compared to their signal level counterpart.

The maximum collector-emitter voltage that a power transistor can withstand in active region is determined by the Base collector avalanche break down voltage. This voltage, denoted by V_{SUS} in Fig, 3.4 is usually smaller than V_{CEO}. The voltage V_{SUS} can be attained only for relatively lower values of collector current. At higher collector current the limit on the "total power dissipation" defines the boundary of the allowable active region as shown in Fig 3.4.

At still higher levels of collector currents the allowable active region is further restricted by a potential failure mode called **"the Second Break down"**. It appears on the output characteristics of the BJT as a precipitous drop in the collector-emitter voltage at large collector currents. The collector voltage drop is often accompanied by significant rise in the collector current and a substantial increase in the power dissipation. Most importantly this dissipation is not uniformly spread over the entire volume of the device but is concentrated in highly localized regions. This localized heating is a combined effect of the intrinsic non uniformity of the collector current density distribution across the cross section of the device and the negative temperature coefficient of resistively of minority carrier devices which leads to the formation of "current filamements" (localized areas of very high current density) by a positive feed-back mechanism. Once current filaments are formed localized "thermal runaway" quickly takes the junction temperature beyond the safe limit and the device is destroyed.

It is in the saturation region that the output characteristics of a Power transistor differs significantly from its signal level counterpart. In fact the saturation region of a Power transistor can be further subdivided into a **quasi saturation region** and a hard saturation region. Appearance of the quasi saturation region in the output characteristics of a power transistor is a direct consequence of introducing the drift region into the structure of a power transistor. In the quasi saturation region the base-collector junction is forward biased but the lightly doped drift region is not completely shorted out by excess minority carrier injection from the base. The resistivity of this region depends to some extent on the base current. Therefore, in the quasi saturation region, the base current still retains some control over the collector current although the value of β decreases significantly. Also, since the resistivity of the drift region is still significant the total voltage drop across the device in this mode of operation is higher for a given collector current compared to what it will be in the hard saturation region.

In the hard saturation region base current looses control over the collector current which is determined entirely by the collector load and the biasing voltage V_{CC}. This behavior is similar to what happens in a signal transistor except that the drift region of a power transistor continues to offer a small resistance even when it is completely shorted out (by excess carrier injection from the base). Therefore, for larger collector currents the collector-emitter voltage drop is almost proportional to the collector current. Manufacturers usually provide the plots of the variation of V_{CE} (sat) vs. i_C for different values of base current and junction temperature. Curves showing the variation of V_{CE} (sat) with i_B for different values of i_C and junction temperature are also provided by certain manufacturers.

Applicable operating limits on a power transistors are compactly represented in two diagrams called the Forward Bias Safe Operating Area (FBSOA) and the Reverse Bias Safe Operating Area. (RBSOA) applicable to $i_B > 0$ and $i_B \leq 0$ conditions respectively. Typical safe operating areas of power transistors are shown in Fig 3.5.

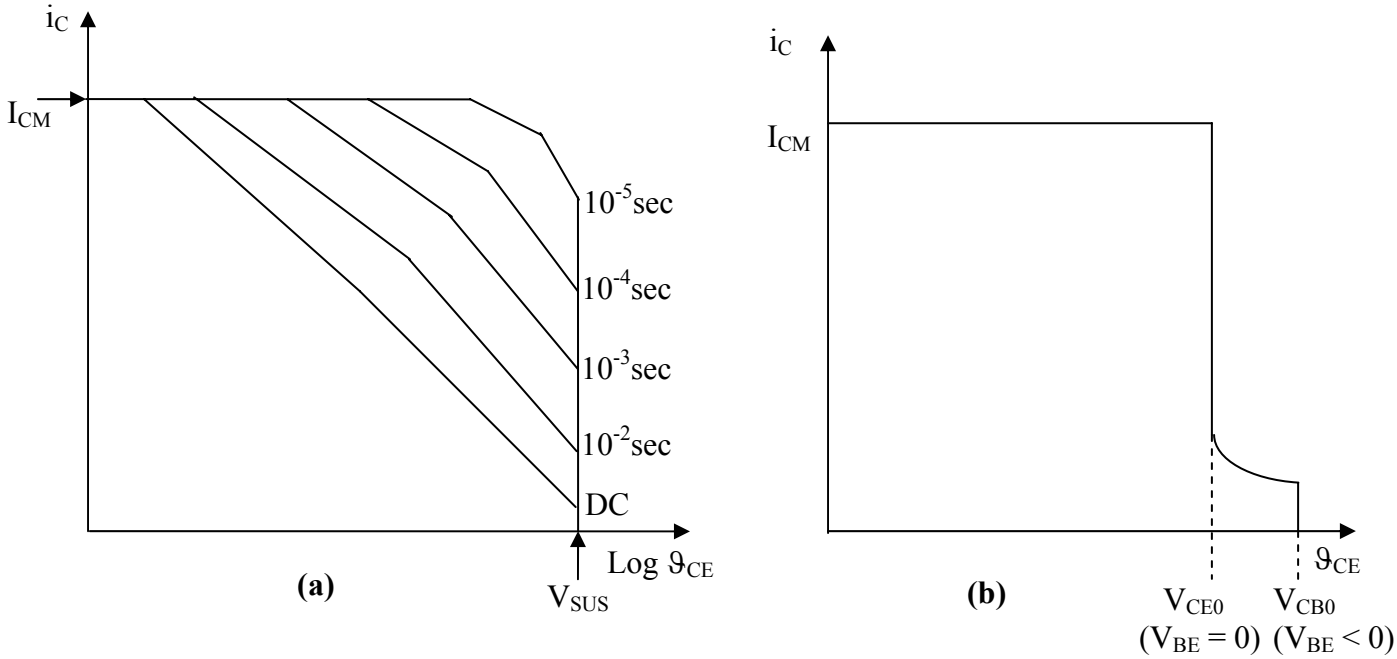


Fig. 3.5: Safe operating areas of a Power Transistor.
(a) FBSOA; (b) RBSOA.

The horizontal upper limit of the FBSOA is determined by the maximum allowable collector current (I_{CM}) that should not be exceeded even as a pulse. Exceeding this current limit may cause bonding wire or metallization of the wafer to vaporize or otherwise fail. Since a power transistor does not have any appreciable reverse voltage blocking capacity they are usually not used in ac circuits. However, if the collector current, for some reason is not dc or a pulse, the rms value of the collector current waveform should not exceed this limit.

The next applicable limit in the FBSOA (green lines) corresponds to the restriction on the maximum allowable power dissipation and maximum junction temperature. Since FBSOA is shown on a log-log scale constant Power dissipation ($P_d = V_{CE}\, i_C$) limits appear as straight lines. This limit is different for dc and pulsed operation due to the thermal time constant of the device. The "DC" limit is applicable to the average power loss if the transistor remains continuously in the conduction state (active, quasi saturation or saturation). On the other hand the pulsed power dissipation limits are applicable to conduction duration up to the value marked on them (the figures on the right of Fig 3.5 (a)). Pulsed power dissipation limits are specified for a low value (1%-2%) of duty cycle and are useful for shaping the switching trajectory of the transistor as will be seen later.

The third limit of the FBSOA (red line) arises due to the **"second break down"** failure mode of a Power transistor. It shows the limiting combinations of collector voltage and current so that second break down does not occur. On the log –log scale of the FBSOA this limit also appears as a straight limit. Like the maximum power dissipation limit, the second break down limit is also different for "DC" and "Pulsed" operation of different pulse durations. The interpretation of the pulse duration (marked on the right side of Fig 3.5 (a)) corresponding to a particular limit is also same.

The final limit of the FBSOA corresponds to the forward biased avalanche break down voltage (V_{SUS}) of the transistor and appear as a vertical line in the FBSOA at $V_{CE} = V_{SuS}$

The FBSOA of a Power transistor is given at a specified case temperature. Both the maximum power dissipation limit and the second break down limits are to be derated as per the derating characteristics provided by the manufacturers when the case temperature exceeds the specified value.

In contrast to the FBSOA, the RBSOA (Fig 3.5 (b)) is plotted on a linear scale and has a more rectangular shape. RBSOA is a switching SOA since a transistor can not conduct current for any appreciable duration under reverse biased condition. It essentially shows the limiting permissible combinations of V_{CE} & i_C with base emitter junction reverse biased. The upper horizontal limit corresponds to the maximum allowable collector current (I_{CM}) and is same as that in the FBSOA. The right hand side vertical limit corresponds the avalanche break down voltage of the transistor with reverse bias. If the base terminal is open (i,e, $i_B = 0$) then this voltage is V_{CEO}. If a negative voltage is applied across the BE junction the right hand side limit of the RBSOA increases somewhat to the value V_{CBO} at low value of the collector current.

In addition to the applicable limits on the output characteristics as represented in the FBSOA and the RBSOA, limiting specification with respect to the base emitter junction is also provided by the manufacturer. Typical specifications that are provided are

V_{EBO} : This is maximum allowable reverse bias voltage across the B-E junction

I_B : Maximum allowable average base current at a given case temperature.

I_{BM} : Maximum allowable peak base current at a given case temperature and of specified pulse duration.

The input characteristics (i_B Vs V_{BE}) at a given case temperature is also provided.

Exercise 3.6

Fill in the blank(s) with the appropriate word(s)

a) In the "Cut off" region collector current of a Power Transistor is _____.
b) In the _____ region of a Power Transistor the dc current gain remains fairly constant.
c) Saturation region of a Power Transistor can be divided into _____ region and _____ region.
d) Active region operation of a Power BJT is limited mostly by _____ consideration.
e) "Second breakdown" in a Power BJT occurs due to _____ of the collector current distribution.

Answer: (a) negligible; (b) active; (c) Quasi saturation, hard saturation; (d) Power dissipation; (e) non uniformity.

3.5 Switching characteristics of a Power Transistor

In a power electronic circuit the power transistor is usually employed as a switch i.e. it operates in either "cut off" (switch OFF) or saturation (switch ON) regions. However, the operating

characteristics of a power transistor differs significantly from an ideal controlled switch in the following respects.

- It can conduct only finite amount of current in one direction when "ON"
- It can block only a finite voltage in one direction.
- It has a voltage drop during "ON" condition
- It carries a small leakage current during OFF condition
- Switching operation is not instantaneous
- It requires non zero control power for switching

Of these the exact nature and implication of the first two has been discussed in some depth in the previous section. The third and fourth non idealities give rise to power loss termed the conduction power loss. In this section the nature and implications of the last two non idealities will be discussed in detail.

Exercise 3.7

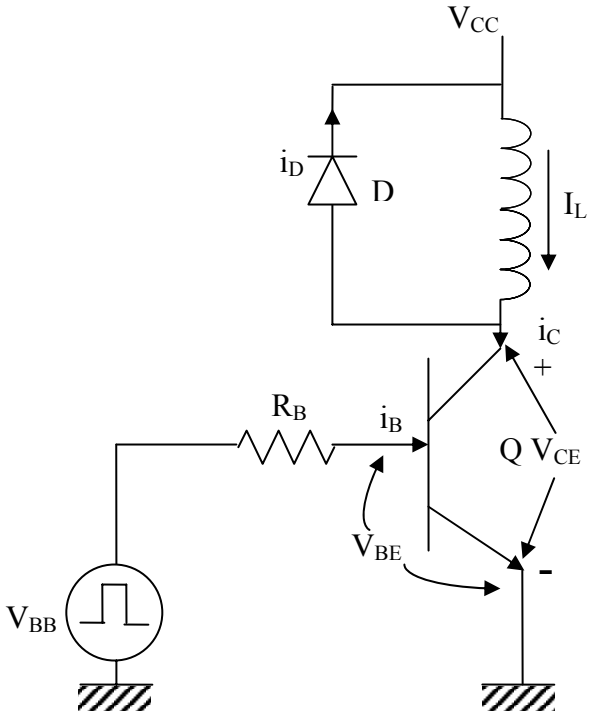
Fill in the blank(s) with the appropriate word(s)

a) An ideal switch can conduct current in _____ directions. While a power transistor conducts current in _____ direction.
b) In power transistor there will be power loss due to ON state _____ and OFF state _____.
c) Unlike an ideal switch the switching of a power transistor is not _____.

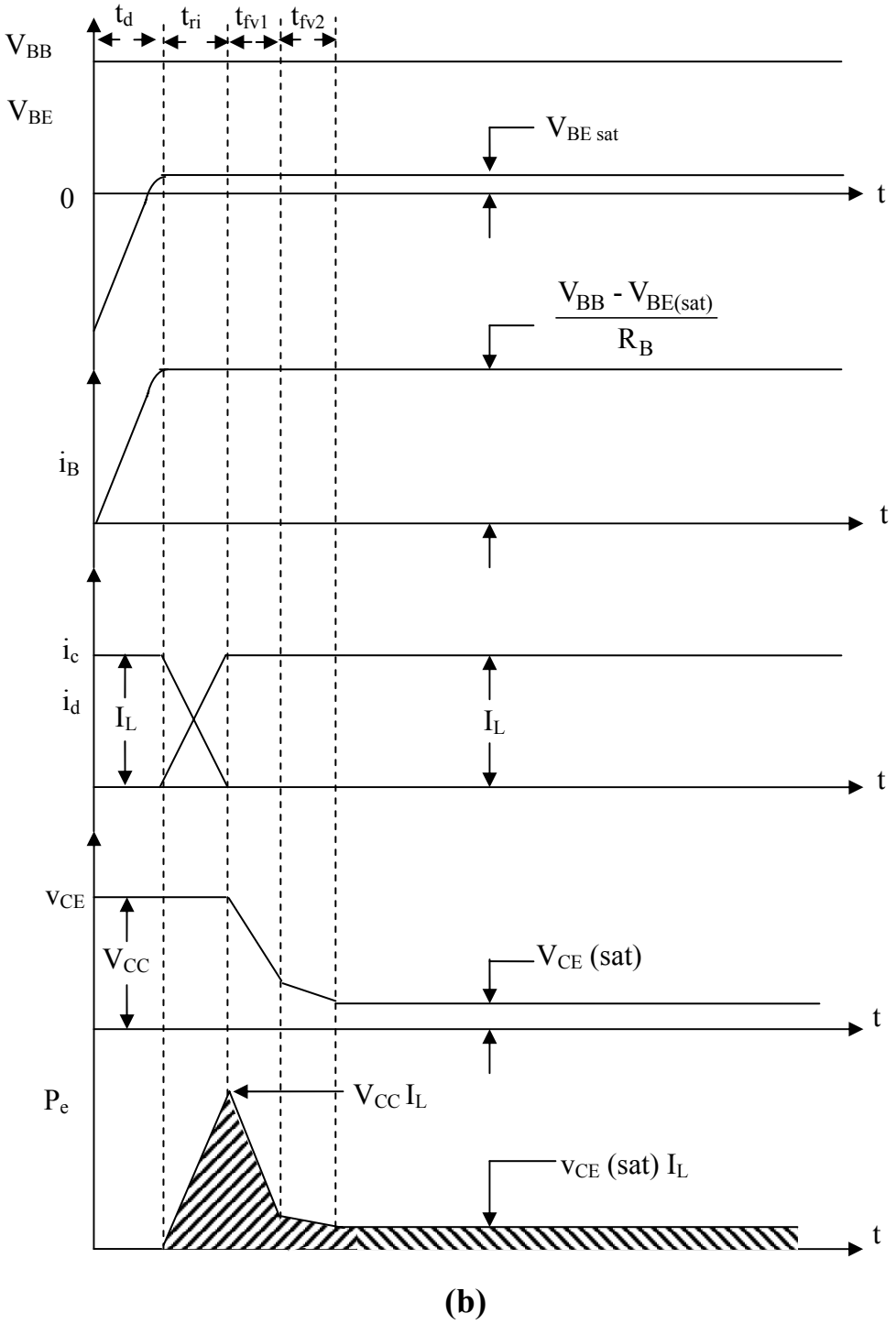
Answer: (a) two, one; (b) voltage drop, leakage current; (c) instantaneous.

3.5.1Turn On characteristics of a Power Transistor

From the description of the basic operating principle of a power transistor presented in the previous sections it is clear that minority carriers must be moved across different regions of a power transistor in order to make it switch between cut off and saturation regions of operation. The time delay in the switching operation of a power transistor is due to the time taken by the minority carriers to reach appropriate density levels in different regions. The exact level of minority carrier densities (and depletion region widths) required for proper switching is determined by the collector current and biasing collector voltage during switching, both of which are determined by external circuits. The rate at which these densities are attained is determined by the base current waveform. Therefore, the switching characteristics of a power transistor is always specified in relation to the external load circuit and the base current waveform as shown in Fig 3.6 which shows a clamped inductive switching circuit with a flat base drive.



(a)



(b)

Fig 3.6 Turn ON characteristics of a power transistor;
(a) Switching circuit, (b) Switching wave forms

The switching wave forms shown in Fig 3.6 (b) are the expanded and to some extent "idealized" version of the actual waveforms that will be observed in a clamped inductive switching circuit as shown in Fig.3.6 (a). Some simplifying assumptions have been made to draw these waveforms. These are

- The load inductor has been assumed to be large enough so that the load current does not change during Turn ON period.
- Reverse recovery characteristics of D has been ignored.
- All parasitic elements have been ignored.

Before t = 0, the transistor (Q) was in the "OFF" state. In order to utilize the increased break down voltage (V_{CBO}) the base-emitter junction of a Power Transistor is usually reverse biased during OFF state. Under this condition only negligible leakage current flows through the transistor. Power loss due to this leakage current is negligible compared to other components of power loss in a transistor. Therefore, it is not shown in Fig 3.6 (b). The entire load current flows through the diode and V_{CE} is clamped to V_{CC} (approximately).

To turn the transistor ON at t = 0, the base biasing voltage V_{BB} changes to a suitable positive value. This starts the process of charge redistribution at the base-emitter junction. The process is akin to charging of a capacitor. Indeed, the reverse biased base emitter junction is often represented by a voltage dependent capacitor, the value of which is given by the manufacturer as a function of the base-emitter reverse bias voltage. The rising base current that flows during this period can be thought of as this capacitor charging current. Finally at $t = t_d$ the BE junction is forward biased. The junction voltage and the base current settles down to their steady state values. During this period, called the "Turn ON delay time" no appreciable collector current flows. The values of i_O and V_{CE} remains essentially at their OFF state levels.

At the end of the delay time ($t_{d\ ON}$) the minority carrier density at the base region quickly approaches its steady state distribution and the collector current starts rising while the diode current (i_d) starts falling. At $t = t_{dON} + t_{ri}$ the collector current becomes equal to the load current (and i_d becomes zero) I_L. At this point D starts blocking reverse voltage and V_{CE} becomes unclamped. t_{ri} is called the current rise time of the transistor.

At the end of the current rise time the diode D regains reverse blocking capacity. The collector voltage V_{CE} which has so far been clamped to V_{CC} because of the conducting diode "D" starts falling towards its saturation voltage V_{CE} (sat). The initial fall of V_{CE} is rapid. During this period the switching trajectory traverses through the active region of the output characteristics of the transistor. At the end of this rapid fall (t_{fv1}) the transistor enters "quasi saturation region". The fall of V_{CE} in the quasi saturation region is considerably slower. At the end of this slow fall (t_{fv2}) the transistor enters "hard saturation" region and the collector voltage settles down to the saturation voltage level V_{CE} (sat) corresponding to the load current I_L. Turn ON process ends here. The total turn on time is thus, $T_{SW}(ON) = t_{d\ (ON)} + t_{ri} + t_{fv1} + t_{fv2}$.

Power loss occurs at all time during the operation of a power transistor. However, the collector leakage current is usually negligibly small and power loss due it can be safely neglected in comparison to the power loss during ON condition. Power loss occurs during Turning ON a Power transistor due to simultaneous existence of non-zero V_{CE} and i_c during t_{ri}, t_{fv1}, and t_{fv2}. The energy lost during these periods is called the Turn ON loss and given by the area under the P_l curve in Fig 3.6 (b). The average Turn ON loss is obtained by dividing this area by ($t_{ri} + t_{fv1} + t_{fv2}$). For safe Turn ON this average power loss must be less than the limit set on the maximum

power dissipation in the FBSOA corresponding to a pulse width greater than $t_{ri} + t_{fv1} + t_{fv2}$. Similar restriction with respect to second break down should also be observed.

Turn ON time can be reduced by increasing the base current. However large base current increases the quantity of excess carrier in the base and collector drift region which has to be removed during Turn Off. As will be seen later this increases the Turn OFF time. The Turn ON delay time can however be reduced by boosting the base current at the beginning of the Turn ON process. This can be achieved by connecting a small capacitance across R_B. This increases the rate of rise of V_{BE} & i_B. Therefore, Turn ON delay time decreases. However, in steady state i_B settle downs to a value determined by R_B & V_{BB} and no adverse effect on the Turn OFF time is observed.

In figure 3.6 (b) the reverse recovery current of D has been neglected. If this current is not negligible then for safe Turn ON operation the sum of the load current and the diode reverse recovery current must be less than the I_{CM} rating of the transistor. Thermal and second break down limits must also be observed.

It should be noted that there is some power loss at the BE junction as well. This power loss depends on the current gain of the transistor during hard saturation. Since current gain reduces during saturation (typically between 5 to 10) this power loss may become significant. Manufacturers usually provide the values of t_d (ON), t_{ri}, t_{fv} as functions of i_c for a given base current and case temperature.

Exercise 3.8

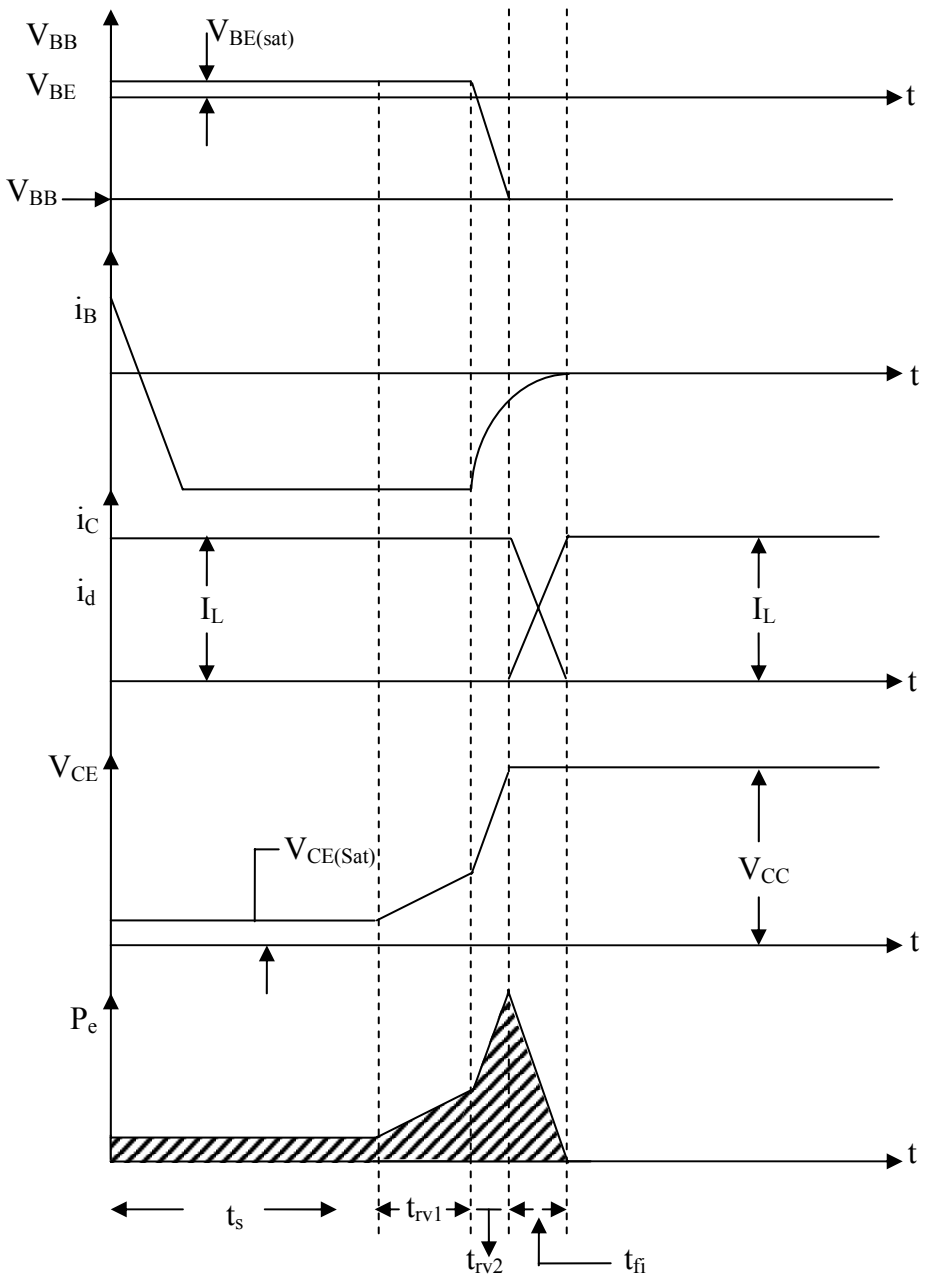
Fill in the blank(s) with the appropriate word(s)

a) For faster switching of a BJT _____ carriers are to be swept quickly from the _____ region.
b) The reverse biased base emitter junction can be represented as a _____ dependent _____.
c) In the quasi saturation region collector-emitter voltage falls at a _____ rate.
d) Turn ON delay can be reduced by _____ the rate of rise of the base current.

Answer: (a) minority, base; (b) voltage, capacitor; (c) slow; (d) increasing.

3.5.2 Turn Off Characteristics of a Power Transistor

During Turn OFF a power transistor makes transition from saturation to cut off region of operation. Just as in the case of Turn ON, substantial redistribution of minority charge carriers are involved in the Turn OFF process. Idealized waveforms of several important variables in the clamped inductive switching circuit of Fig. 3.6 (a) during the Turn OFF process of Q are shown in Fig 3.7 (a)


V_{BB}
$V_{BE(sat)}$
V_{BE}
t
V_{BB}
i_B
t
i_C
i_d
I_L
I_L
t
V_{CE}
$V_{CE(Sat)}$
V_{CC}
t
P_e
t
t_s
t_{rv1}
t_{rv2}
t_{fi}

(a)

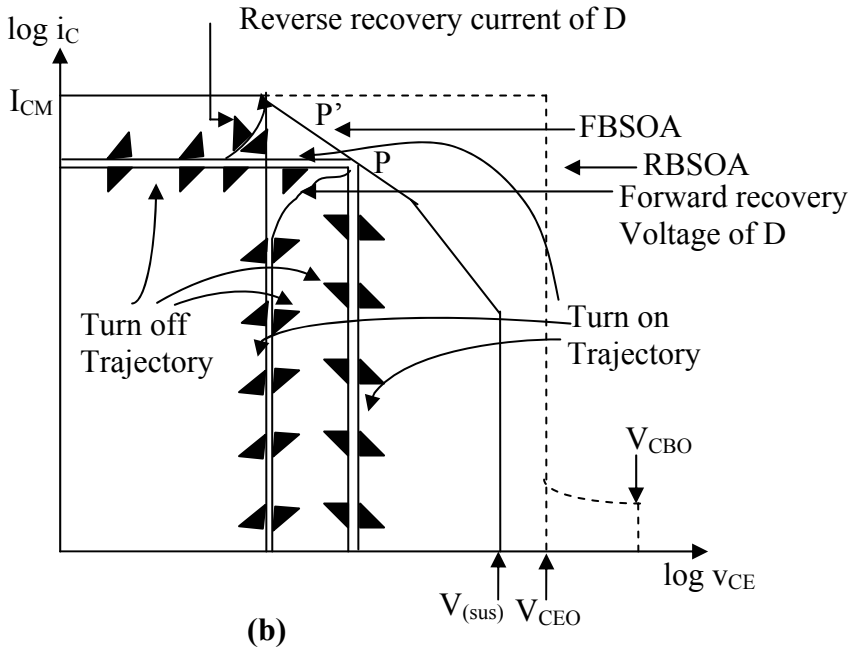


Fig. 3.7: Turn off, characteristics of a BJT.
(a) Switching wave forms
(b) Switching trajectory

The "Turn OFF" process starts with the base drive voltage going negative to a value $-V_{BB}$. The base-emitter voltage however does not change from its forward bias value of $V_{BE}(sat)$ immediately, due to the excess, minority carriers stored in the base region. A negative base current starts removing this excess carrier at a rate determined by the negative base drive voltage and the base drive resistance. After a time "t_s" called the storage time of the transistor, the remaining stored charge in the base becomes insufficient to support the transistor in the hard saturation region. At this point the transistor enters quasi saturation region and the collector voltage starts rising with a small slope. After a further time interval "t_{rv1}" the transistor completes traversing through the quasi saturation region and enters the active region. The stored charge in the base region at this point is insufficient to support the full negative base current. V_{BE} starts falling forward $-V_{BB}$ and the negative base current starts reducing. In the active region, V_{CE} increases rapidly towards V_{CC} and at the end of the time interval "t_{rv2}" exceeds it to turn on D. V_{CE} remains clamped at V_{CC}, thereafter by the conducting diode D. At the end of t_{rv2} the stored base charge can no longer support the full load current through the collector and the collector current starts falling. At the end of the current fall time t_{fi} the collector current becomes zero and the load current freewheels through the diode D. Turn OFF process of the transistor ends at this point. The total Turn OFF time is given by $Ts_{(OFF)} = t_s + t_{rv1} + t_{rv2} + t_{fi}$

As in the case of "Turn ON" considerable power loss takes place during Turn OFF due to simultaneous existence of i_c and V_{CE} in the intervals t_{rv1}, t_{rv2} and t_{fi}. The last trace of Fig 3.7 (a) shows the instantaneous power loss profile during these intervals. The total energy last per turn off operation is given by the area under this curve. For safe turn off the average power dissipation during $t_{rv1} + t_{rv2} + t_{fi}$ should be less than the power dissipation limit set by the FBSOA corresponding to a pulse width greater than $t_{rv1} + t_{rv2} + t_{fi}$.

Turn OFF time intervals of a power transistor are strongly influenced by the operating conditions and the base drive design. Manufacturers usually specify these values as functions of collector current for given positive and negative base current and case temperatures. Variations of these time intervals as function of the ratio of positive to negative base currents for different collector currents are also specified.

In this section and the precious one inductive load switching have been considered. However, if the load is resistive. The freewheeling diode D will not be used. In that case the collector voltage (V_{CE}) and collector current (i_c) will fall and rise respectively together during Turn ON and rise and fall respectively together during Turn OFF. Other characteristics of the switching process will remain same. The switching Power loss in this case will also be substantially lower.

Exercise 3.9

Fill in the blank(s) with the appropriate word(s)

a) Turn OFF process in a BJT is associated with transition from the _____ region to the _____ region.
b) Negative _____ current is required to remove excess charge carriers from the _____ region of a BJT during Turn OFF process.
c) V_{CE} increases rapidly in the _____ region.

Answer: (a) Saturation, Cut-off; (b) base, base; (c) active.

3.5.3 Switching Trajectory and Switching Losses in a Power Transistor

It has been mentioned in the earlier sections that energy loss takes place in a power transistor during each switching operation. Instantaneous power loss during switching can be calculated and plotted as shown in Fig 3.6 (b) and 3.7 (a). The areas under these curves indicate the energy loss during each switching operation (Turn ON and Turn OFF). Indicating these areas as E_{ON} and E_{OFF} during Turn ON and Turn OFF operations respectively one can write.

$$E_{ON} = \frac{1}{2}\left[V_{CC} I_L \, t_{ri} + \left(V_{CC} + V_{CEfl}\right) I_L t_{fv1} + \left(V_{CEfl} + V_{CE(sat)}\right) I_L t_{fv2} \right] \quad (3.5)$$

Where V_{CEfl} is the value of V_{CE} at the end of the interval t_{fv1}

Similarly

$$E_{OFF} = \tfrac{1}{2}\left[\left(V_{CE}\,(sat) + V_{CEr1}\right) I_L t_{rv1} + \left(V_{CEr1} + V_{CC}\right) I_L t_{rv2} + V_{CC} I_L t_{fi} \right] \quad (3.6)$$

If the switching frequency of the transistor is f_{SW}, then the average switching power loss is given by

$$P_{SW} = \left(E_{ON} + E_{OFF}\right) f_{SW} \qquad (3.7)$$

On the other hand the conduction energy loss is given by the area hatched black in Fig 3.6 (b) and 3.7(a). From these figures the conduction power loss is given by

$$P_C = V_{CE}(sat) I_L \left(T_{ON} - t_d(ON) - t_{ri} - t_{fv1} - t_{fv2} + t_s\right) f_{SW} \quad (3.8)$$

Where T_{ON} is the time period for which the base drive voltage remain positive. Usually $t_s - T_{SW}(ON) << T_{ON}$, Therefore

$$P_C = V_{CE}(sat) I_L \; T_{ON} \, f_{SW} = V_{CE}(sat) I_L D \quad (3.9)$$

Where D is the switching duly cycle.

For a given V_{CC} and I_L and base drive design, E_{ON} and E_{OFF} are constant. Therefore, the switching power loss is proportional to the switching frequency. Being a minority carrier device a BJT has comparatively larger switching times (compared to some other devices broadly categorized as transistors) and hence larger switching power loss for a given frequency. On the other hand a BJT has the lowest ON state voltage drop V_{CE} (sat) among all fully controlled switches. Therefore, a BJT is suitable for switching large current at moderate (around a few KHZ) switching frequency. At high frequency BJT based circuits tend to become inefficient due to increased switching power loss.

Even without any restriction on the switching power loss the maximum switching frequency of a BJT is limited by its Turn ON and Turn OFF times. The value of the maximum switching frequency is given by

$$F_{SW}(Max) = \frac{1}{T_{SW}(ON) + T_{SW}(OFF)} \quad (3.10)$$

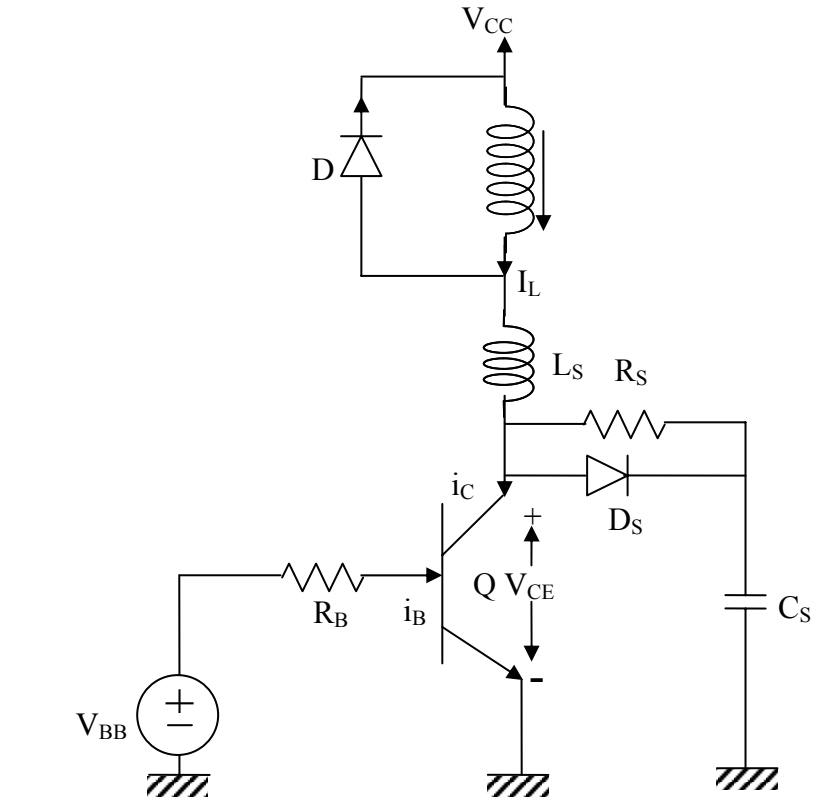
For a given collector current and base drive design.

For safe switching operation, however it is not sufficient to merely restrict the switching power loss. It will be necessary to restrict the switching trajectory (an instantaneous plot of i_c vs V_{CE} during switching with time as a parameter) within the FBSOA /RBSOA region corresponding to a pulse width greater than T_{SW} (ON) or T_{SW} (OFF). Fig 3.7 (b) shows these switching trajectories superimposed on the FBSOA /RBSOA. In this diagram the green line corresponds to the Turn ON trajectory while the blue line corresponds to the Turn OFF trajectory. These trajectories are rectangular in nature. Clearly full voltage (V_{CEO}) or current rating (I_{CM}) of the transistor can not be utilized in such a trajectory. The situation becomes worse a when the reverse recovery current and forward recovery voltage of D is considered. **Switching aid circuits or "snubbers"** (as they are popularly known) are used to enhance the switching performance of a power transistor. They serve two specific purpose.

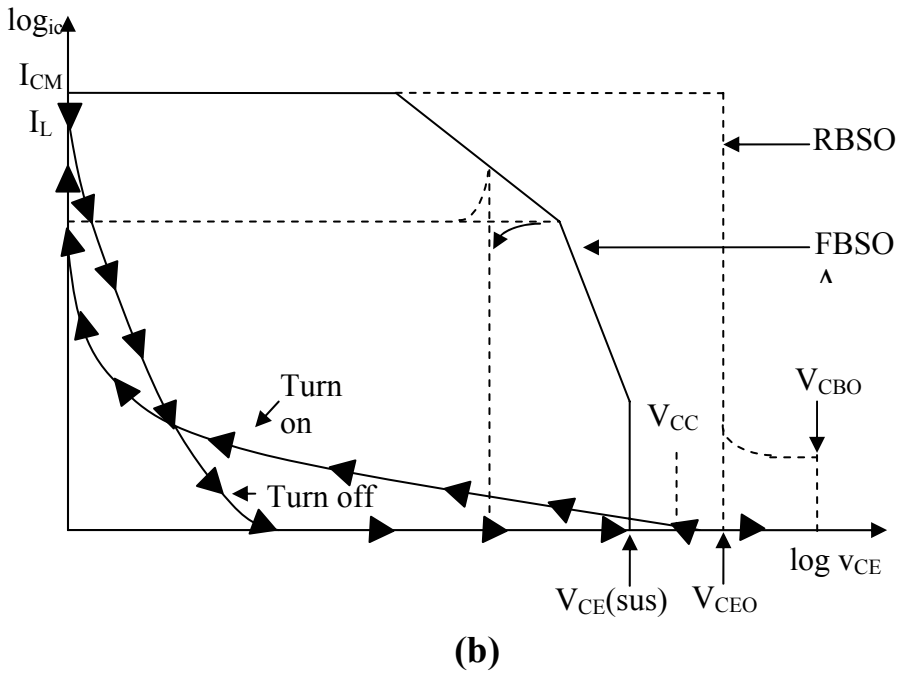
- Shape the switching trajectory such that the voltage and current rating of a transistor can be fully utilized.

- Reduce the switching power loss inside the device.

Fig. 3.8 shows a typical snubber circuit for a power transistor and the corresponding switching trajectories.



(a)



(b)

Fig. 3.8: Switching characteristics of a BJT with Snubber
(a) Clamped inductive switching circuit with snubber
(b) Switching trajectory.

Fig 3.8 (a) shows the same clamped inductive switching circuit of Fig 3.6 (a) but with the snubber elements. The inductor L_S connected between the load and the collector is the Turn ON snubber. In decouples the collector from the supply voltage during Turn ON. Therefore, as the junction V_{BE} becomes forward biased V_{CE} starts falling. At the same time i_c also starts rising towards I_L. The resultant switching trajectory is shown by the solid green line in Fig 3.8 (b). This should be compared with the unsnubbed Turn ON trajectory (broken green line). In the unsnubbed case, the collector current rises to the maximum value before V_{CE} starts falling from V_{CC}. $V_{CC,}$ therefore, must necessarily be smaller than V_{CE} (SUS). In the snubber assisted trajectory V_{CE} falls substantially before i_c rises to any appreciable value. Therefore, V_{CC} can be made larger than $V_{CE}(sat)$ and can be chosen closer to V_{CEO}. Maximum collector current that can be handled is also considerably higher $\left(I_{L|Max} = I_{CM} - I_{rr}(D)\right)$. In the unsnubbed case maximum I_L is restricted essentially by the maximum power dissipation consideration and not by I_{CM}. L_S also helps to reduce I_{rr} (D) by restricting the rate of decrease of current through D. This also helps to increase $I_{L|Max}$

Rs-Cs-Ds constitute the Turn OFF snubber. This is popularly known as the "R-C-D snubber". During Turn OFF as the base drive of Q is removed i_c starts falling and the remaining load current is bypassed to Cs through D_s. Therefore, the collector voltage rises simultaneously giving rise to the Turn OFF trajectory shown by the solid blue line in Fig 3.8 (b). At the end of the Turn OFF process V_{CE} shoots over V_{CC} due to L_s-C_s oscillation. However, by proper design $V_{CE|Max}$ can be restricted well below V_{CBO}. Therefore, the turn OFF snubber circuit can effectively utilize the enhanced voltage withstanding capability of a power transistor with base reverse biased.

Comparison of the switching trajectories with and with out snubber circuit makes it evident that the snubber circuit can considerably enhance the voltage and current capacity utilization of a Power transistor.

The area enclosed under the switching trajectories is a measure of the switching loss occurring in the device at each switching. Therefore, it is evident from Fig 3.8 (b) that the snubber circuit reduces the switching power loss inside the device considerably. However, it should be emphasized that the total switching loss (device + snubber resistance) may not reduce. It is also necessary to place the snubber components very close to the transistor since any stray inductance in the Rs – Cs – Ds loop may give rise to an unacceptably large voltage spike across Q. Components should also be chosen very carefully. Rs must be non inductive and the lead inductances of Ds and Cs must be kept to a minimum Power loss in Rs can be considerably large and its wattage should selected accordingly. To avoid excessive power loss in Rs, lossless (regenerate) snubber circuits have been proposed.

Exercise 3.10

Fill in the blank(s) with the appropriate word(s)

a) BJT has large switching times, since it is a _____ carrier device.
b) BJT has _____ ON state voltage drop.
c) BJT is inefficient at _____ switching frequencies.

d) Turn OFF snubber circuit is used to improve _____ withstand capacity of a BJT.

Answer: (a) minority; (b) low; (c) high; (d) voltage.

Exercise 3.11

What are the effects of introducing a drift region in the output i-v characteristics of a power transistor?

Answer: The drift region in a power transistor is introduced in order to block large forward voltage. However, one effect of introducing the drift region is the appearance of a "quasi saturation region" in the output i-v characteristics of a power transistor. In the quasi saturation state the drift region is not completely shorted out by "conductivity modulation" by excess carriers from the base region. In offers a resistance which is a function of the base current. Although the base current retain some control over collector current in this state the value of dc current gain reduces substantially due to increased effective base width.

Another effect of introducing the drift region is to make the V_{CE} saturation voltage depend linearly on the collector current in the hard saturation region due to the ohmic resistance of the "conductivity modulated" drift region.

Exercise 3.12

Explain the importance of the following manufacturer's specifications
(a) FBSOA, (b) β vs i_c characteristics, (c) i_B vs V_{BE} characteristics

Answer: (a) FBOSOA compactly represents the safe operating limits of a power transistor in terms of maximum forward current, maximum forward voltage, maximum average & instantaneous power dissipation and second break down limits. It is most useful in designing the switching trajectory of a power transistor.

(b) This characteristics gives the amount of base current required so that the transistor can operate in the saturation mode for a given collector current.

(c) After the base current is determined, this characteristics is used to design the base drive circuit for a given base power source.

3.5.4 Base Drive Design and Power Darlington

The performance of a Power transistor depends largely on the base drive design.

- The rate of rise of base current in the beginning of the turn on process determines the turn on delay time.
- The magnitude of the base current during turn on decides the values of the voltage fall time, current rise time and V_{CE} (sat) for a given collector current.

- The negative base current during turn off determines the storage time, voltage rise time and current fall time.
- A negative bias at the base also enhances the voltage withstanding capacity of a power transistor.

From the discussion of the switching characteristics of a BJT it is evident that the base drive voltage source should be bipolar and the base drive resistance should be different during turn on and turn off. The following step by step procedure can be followed to arrive at the values.

- From the load current value (to be switched) and desired conduction power loss the desired value of V_{CE} (sat) is determined.
- Using the desired value of V_{CE} (sat) for the given load current, the required value of forward base current (i_{BP}) and the corresponding V_{BE} (sat) is obtained from the manufacturer's data sheet.
- The forward and reverse base drive voltages (V_{BB} + & V_{BB} -) are decided on the basis of the availability of control power supply. These should be kept as low as possible in order to reduce base drive power requirement.
- The forward base drive resistance R_{BP} is given by

$$R_{BP} = \frac{V_{BB+} - V_{BE}(sat)}{i_{BP}} \qquad (3.11)$$

It has been mentioned earlier that the turn on delay time can be reduced by increasing the rate of rise of i_{BP} at the beginning of the turn ON process. This is achieved by connecting a small capacitor across R_{BP}.

- Once i_{BP} is known the turn on loss is fixed. The allowable turn off loss is determined by subtracting the turn on loss for the desired total switching loss. The required current fall and voltage rise times for the calculated turn off loss is determined for the given load current and V_{CC}.
- A suitable negative base current (i_{BN}) to give the desired voltage rise time is determined from the manufacturer's data sheet.
- R_{BN} is given

$$R_{BN} = \frac{V_{BB-} + V_{BE}(sat)}{i_{BN}} \qquad (3.12)$$

- Once i_{BN} is fixed the storage time (ts) can be determined from the manufacturer's data sheet.
- The storage time can be reduced by connecting a small capacitor across R_{BN}.

The resulting base drive circuit can be realized as shown in Fig 3.9

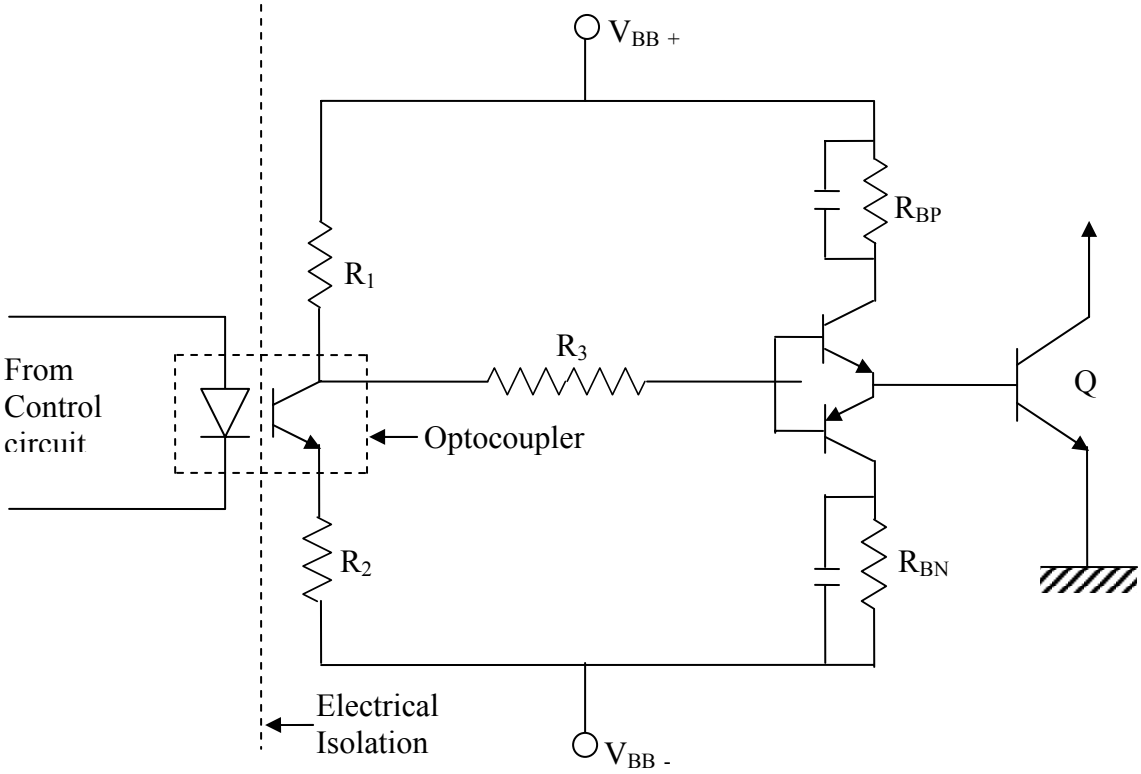
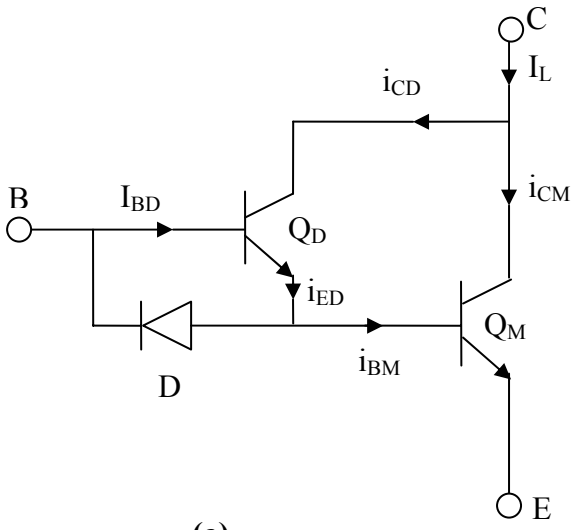


Fig 3.9: Typical base drive circuit of a power transistor

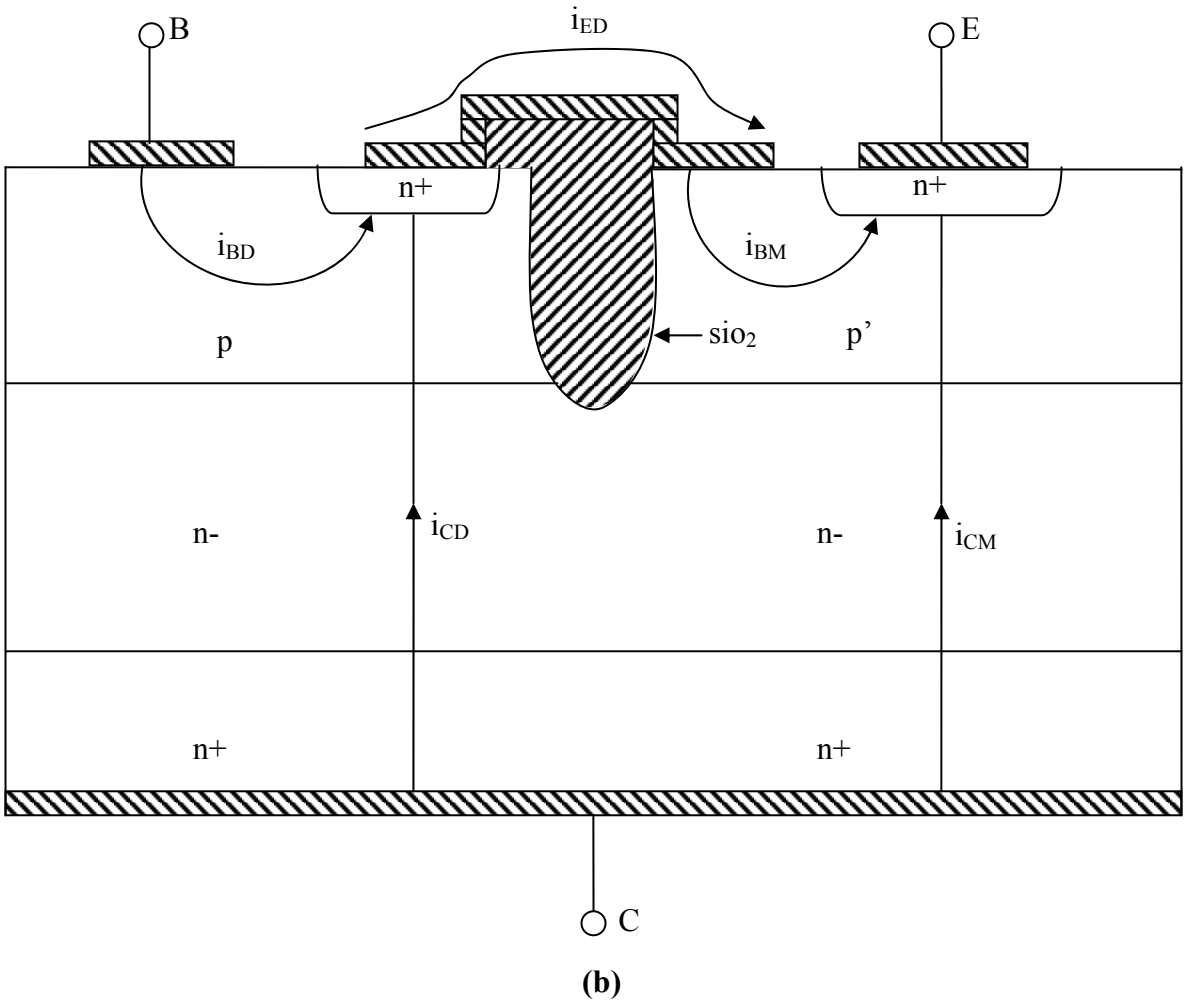
Power transistors have low values of dc current gain (β) compared to their signal level counterpart. Particularly, if a low value of V_{CE} (sat) is desired at full load current, β can be as low as 5. With such low gain large current switching becomes difficult since the base drive circuit is required to handle about 20% of the full load current, Monolithic, Darlington connected transistors can solve this problem. Fig 3.10 shows the circuit connection and the vertical cross section of a Monolithic Darlington pair. The effective current gain of a Darlington pair is given by

$$\beta = \beta_M \beta_D + \beta_M + \beta_D \qquad (3.13)$$

So that even when individual β's are small effective β can still be quite large.



(a)



(b)

Fig 3.10: Monolithic Darlington connected power transistor.
(a) circuit diagram, (b) schematic cross section.

In the Darlington configuration the base drive current for the main transistor is derived from the collector biasing power supply through a drive transistor. This drive transistor should have the same voltage rating as the main transistor but lower current rating. In a monolithic design both are fabricated from the same crystal. The silicon protrusion through the **p** layer (the base region for both transistors) isolates the two bases from each other. A discrete diode D is added (Fig 3.10 (a)) to speed up the turn off time of the main transistor.

The major quantitative difference in the operating characteristics of a Power Darlington is due to the fact that the main transistor can not go into hard saturation. The ON state voltage drop of the drive transistor prevents forward biasing of the C-B junction of the main transistor. Therefore, the ON state power dissipation of the main transistor will be larger than that of an otherwise comparable single BJT. The switching times will also be somewhat larger for the Darlington transistor.

Exercise 3.13

A Power BJT is used to switch an inductive load carrying 20 A. The supply voltage is 200V, switching frequency and duty cycle are 1 KHZ and 0.5 respectively. Switching times are as follows. $t_d = 1\mu s$, $t_{ri} = t_{fv1} = 8\ \mu s$, $t_{fv2} = 0$, $t_s = 12\ \mu s$, $t_{fi} = t_{rv2} = 8\ \mu s$, $t_{rv1} = 0$. $V_{CE}\big|_{sat} = 1.0V$ at $i_c = 20\ A$

Calculate switching and conduction losses in the transistor.

Answer: Turn on energy loss is given by.

$$E_{ON} = \frac{1}{2} V_{CC} I_L \left(t_{ri} + t_{fv1}\right) = 32\ mJ$$

Turn off energy loss is given by

$$E_{off} = \frac{1}{2} V_{CC} I_L \left(t_{fi} + t_{rv2}\right) = 32mJ$$

So total energy loss per switching = $E_{ON} + E_{0ff} = 64$ mJ.

$\therefore$ Switching power loss = $f_{sw}\ (E_{ON} + E_{off}) = 64$ watts.

Conducting loss per switching is given by

$$E_{COND} = I_L\ V_{CE}\big|_{sat} \left(\frac{D}{f_{SW}} - t_d - t_{ri} - t_{fv} + t_s\right) = 9.9\ mJ$$

$\therefore$ Conduction power loss = 9.9 watts.

Exercise 3.14

With reference to Fig. 3.9 determine the values of the base resistors R_{BP} & R_{BN} for the following data

$V_{BB+} = 10$ volts, $V_{BB-} = -10$ V, $I_{BP} = 2.5$ A, $I_{BN} = 1.5$ A, $V_{BE}\big|_{sat} = 0.7\ V$, $V_{CE}\big|_{sat}$ (of drive transistors) = 0.3 V

Answer: $R_{BP} = \frac{V_{BB} + - V_{BE}\big|_{sat} - V_{CE}\big|_{sat}}{I_{BP}} = 3.6\,\text{ohms.}$

$R_{BN} = \frac{V_{BE}\big|_{sat} - V_{CE}\big|_{sat} - V_{BB-}}{I_{BN}} = 6.93\,\text{ohms}$

References

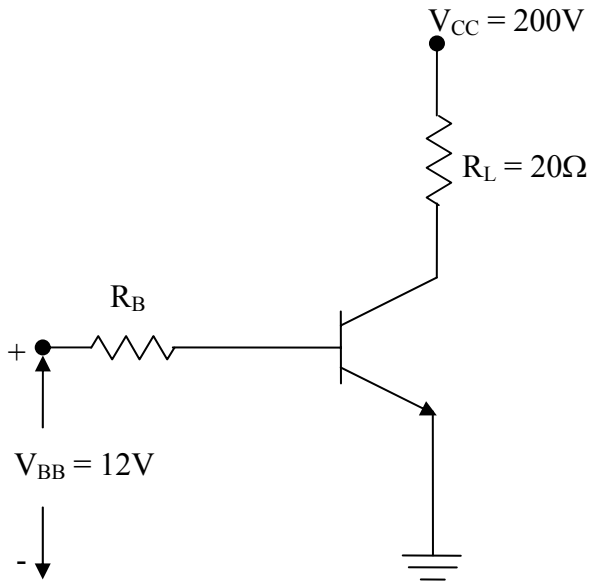
1) Jacob Millman, Christos C. Halkis, “Integrated Electronics, Analog and Digital circuit and systems”, Tata McGrow-Hill publishing Company Limited, New Delhi, 1991.
2) Ned Mohan, Tore M. Undeland, William P. Robbins, “Power Electronics, Converters, Application and Design”. John Willey & Sons (Asia) Publishers, Third Edition, 2003.

Lesson Summary

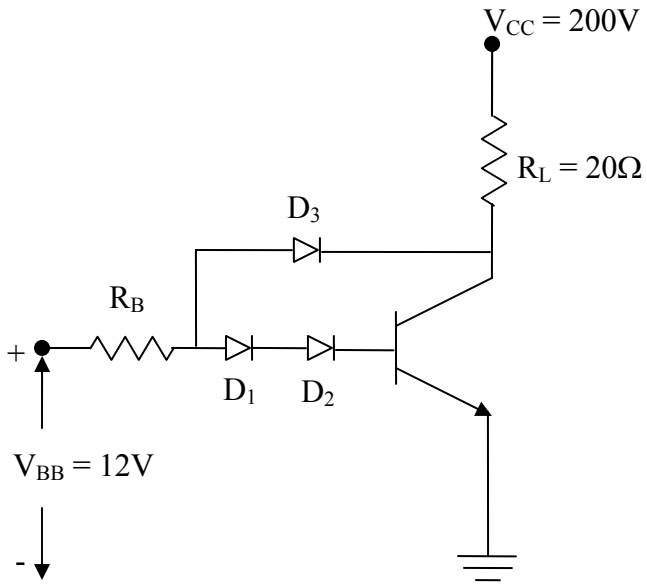
- A Bipolar Junction Transistor is a minority carrier, current controlled unidirectional device.
- A BJT can be of **n-p-n** or **p-n-p** type with three terminals called the collector, the base and the emitter.
- A BJT can operate in cut-off, active or saturation regions.
- In the cut-off region the base emitter junction is reverse biased and the collector current is almost zero.
- In the active region the ratio of collector current to base current is fairly constant. This ratio is called the dc current gain (β).
- A transistor can be driven into saturation by increasing the base current for a given collector current. In saturation the V_{CE} voltage drop of a transistor is very low.
- For power application normally, **n-p-n** type transistor in the common emitter configuration with the base as the control terminal is used. They operate either in the cut-off, or saturation mode.
- For safe operation power transistors must observe maximum current, maximum voltage, maximum power dissipation and second break down limits.
- Operating restrictions applicable to a power transistor under forward and reverse bias conditions are represented compactly in FBSOA & RBSOA diagrams respectively.
- Power transistor output i-v characteristics exhibits a quasi saturation region not found in their signal level counterpart. It is the direct consequence of introducing a lightly doped n^- drift region in the structure of a power transistor which enhances its forward voltage blocking capacity.
- Switching of Power transistors from ON (saturation) to OFF (cut-off) state involves considerable redistribution of minority carriers. Therefore, switching operation is not instantaneous.
- Switching characteristics of a power transistor is greatly influenced by the external load circuit and the base drive circuit.
- Energy loss takes place during each switching operation of a power transistor due to simultaneous existence of collector current and voltage. This is called switching loss.
- Energy loss taking place during ON condition of the transistor is called the conduction loss. Conduction loss during the OFF state of a Power transistor is negligibly small.
- Switching power loss is proportional to the switching frequency while the conduction power loss is proportional to the duly cycle.
- BJT being a minority carrier device have low on state voltage drop and longer switching delay times compared to some “majority” carrier “transistors”. Consequently, BJT has higher switching loss and lower conduction loss.
- A Power transistor is suitable for large current switching at low to moderate (a few kHZ) frequency.

- Switching aid circuits (snubbers) are used for enhancing the capacity utilization of a power transistor. They also reduce switching loss internal to the device.
- Ordinary L-R-C-D snubber circuits may not reduce total switching loss. For that purpose lossless (regenerative) snubber circuits are used.
- Proper design of the base drive circuit helps to reduce both conduction and switching losses. For optimal operation, base drive voltage should be bipolar and have different output resistance for Turn ON and Turn OFF operations.
- Power transistors have relatively small current gain (β) and hence require large base drive current.
- Monolithic Power Darlingtons can solve the problem of low current gain. But they have larger ON state voltage drop and longer switching times.

Practice Problems and Answers

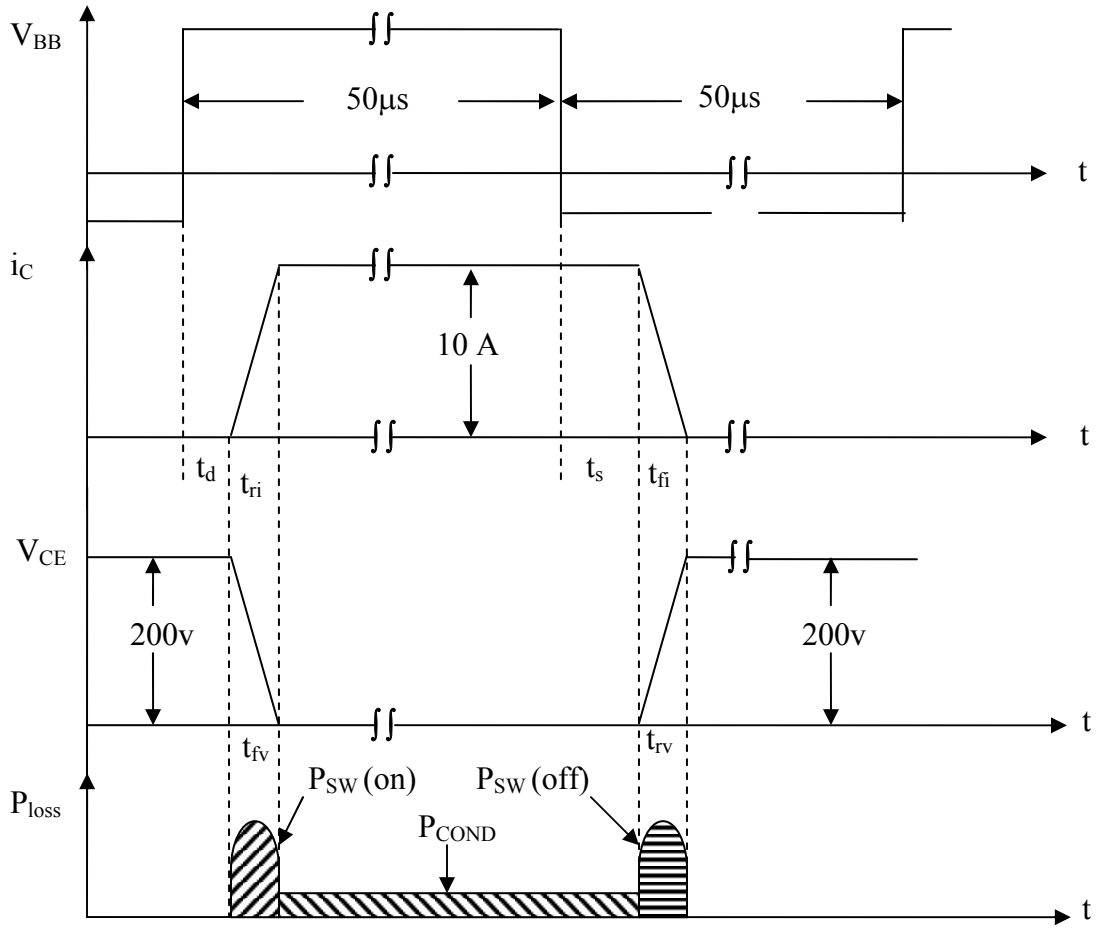


1. In the transistor switching circuit $V_{BE}\big|_{sat} = 0.75\ V,\ V_{CE}\big|_{sat} = 0.2\ V\ \ 10 \le \beta \le 40$.
   Find out the value of R_B and Power requirement of the base source.



2. In the transistor switching circuit shown
   $V_{BE}\big|_{sat} = 0.75$ v, $V_{D1} = V_{D2} = V_{D3} = 0.7$ v, $\quad 10 \le \beta \le 40$
   Find maximum allowable value of R_B and power output of the base source. Also compare conduction power loss with the circuit shown in Problem – 1.

3. The transistor of Problem -1 has the following switching time specifications.
   $t_d = 1\mu s$, $t_{ri} = t_{fv} = 2.5\ \mu s$, $t_s = 5\ \mu s$, $t_{fi} = t_{rv} = 2.5\ \mu s$. The transistor is switched at a frequency of 10 KHZ with duty ratio d = 0.5. Find out, (i) conduction power loss, (ii) switching power loss.



4. Figure shows practical implementation of a power transistor base drive circuit. The comparator has an output voltage swing of ± 12 V.
   Also

   For Q_P

   $V_{BE}\big|_{sat} = 0.7V,\ V_{CE}\big|_{sat} = 0.2V,$

   For Q_N

   $V_{BE}\big|_{sat} = -0.7\,V,\ V_{CE}\big|_{sat} = -0.2\,V,$

   For Q

   $V_{BE}\big|_{sat} = 0.75\,V.\ \beta\big|_{Min} = 10.$ Also it is desired that negative base current should be at least equal to positive base current. $\beta\big|_{Min}$ of Q_P & Q_N are same. Find the values of R_{BP}, R_{BN} and R_1

5. Explain why the dc current gain of a Power BJT is considerably lower compared to its Signal level counterpart. What adverse effect does it have on the switching performance of a BJT? Suggest one solution to this problem.

6. Differentiate between the voltage ratings V_{SUS}, V_{CEO} & V_{CBO} of a Power BJT. How can these three voltage ratings of a BJT be utilized in an inductive switching circuit.

7. The pulsed FBSOA of a Power BJT is usually specified for a very low duty cycle. Then now does it help to extend the usable voltage and current rating of a BJT?

Answer to Test Problems

1. The load current $I_L = i_c = \frac{200 - V_{CE}|_{sat}}{20} \approx 10$ Amps

$V_{CE}|_{sat} = 0.2V,$ which indicates that the transistor is in hard saturation. Therefore $\beta = \beta_{min} = 10$.

So required base current $= i_c/10 = 1$ amps

$V_{BE}|_{sat} = 0.75$ volts $\quad \therefore R_B = V_{BB} - V_{BE}|_{sat} = 11.25\,\Omega$

Power drawn from base source is $12 \times 1 = 12$ watts.

2. In this case $V_{CE} = V_{BE}|_{sat} + V_{D2} + V_{D1} - V_{D3} = 1.45$ volts . The transistor is not in saturation since V_{CB} is positive. So $\beta = \beta_{max} = 40$

$I_L = i_c = \frac{200 - 1.45}{20} = 9.93$ Amps.

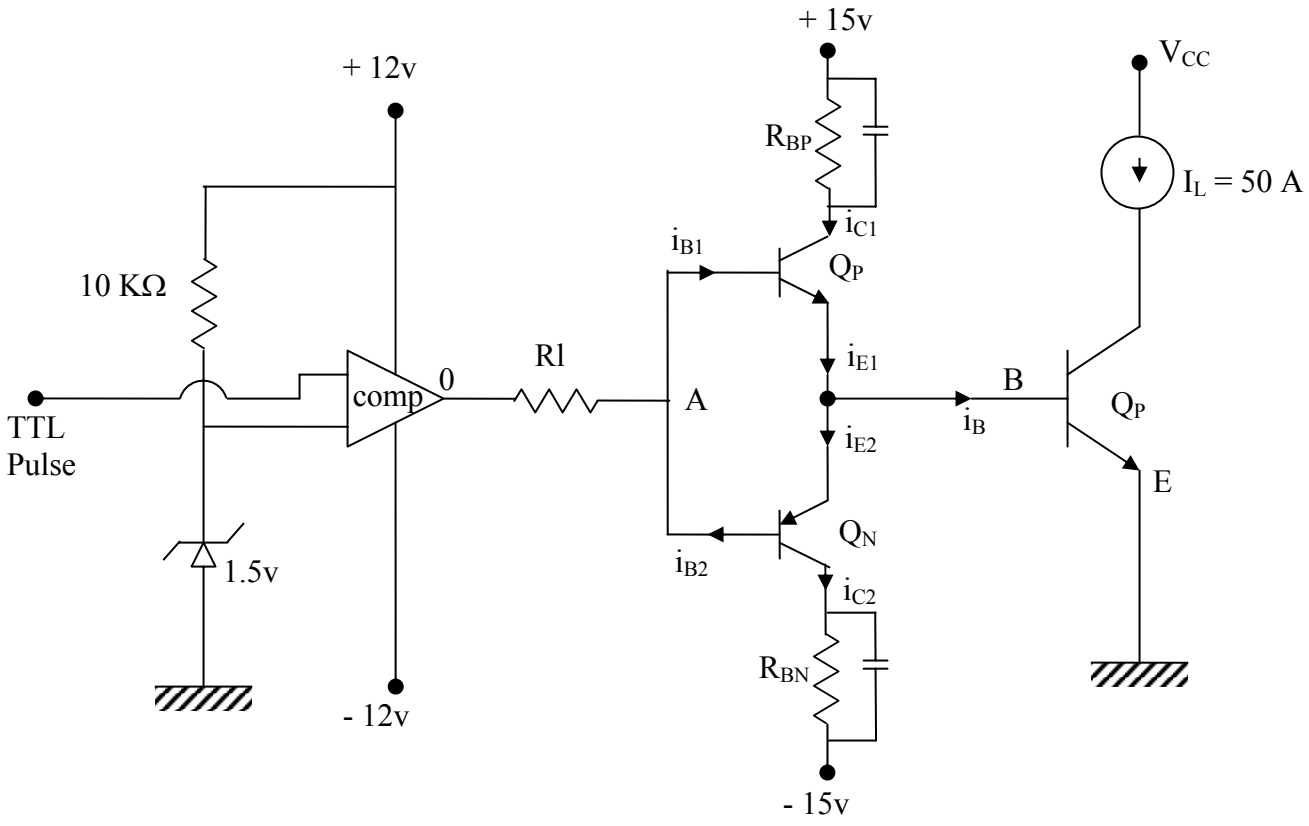
$\therefore i_B = i_c/\beta = 0.25$ Amps.

For maximum value of R_B current through D_3 will be zero

So $R_B = \frac{V_{BB} - V_{D1} - V_{D2} - V_{BE}|_{sat}}{i_B} = 39.4\,\Omega$

Power Drawn from base source is $12 \times 0.25 = 3$ watts.
Conduction power lass in 1st problem was $10 \times 0.2 = 2$ watts
Conduction power lass in this case is $9.93 \times 1.45 = 14.4$ watts

Note: This circuit is known as the anti-saturation clamp or the “Baker’s clamp”.



3. Figure shows switching waveforms of the transistor. Major difference with clamped inductive switching waveform is that in this case rise and fall of i_c & V_{CE} are simultaneous. In the interval t_{ri} $(\text{or } t_{fv})$

$$i_c = 10\frac{t}{t_{ri}} = 4\times10^6\, t$$

$$V_{CE} \approx 200\left(1 - t/t_{fv}\right) = 200\left(4\times10^5\, t\right).$$

where $V_{CE}\big|_{sat}$ has been neglected.

In the interval t_{fi} $(\text{or } t_{rv})$

$$i_c = 10\left(1 - t/t_{fi}\right) = 10\left(1 - 4\times10^5\, t\right)$$

$$V_{CE} = 200\ t/t_{rv} = 80\times10^6\, t$$

$$\therefore E_{SW}(ON) = \int_o^{t_{ri}} V_{CE}\, i_c\, dt$$

$$= \int_o^{2.5\times10^6} 8\times10^8\, t\left(1 - 4\times10^5 t\right) dt$$

$$= 0.83\ \text{mJ}$$

$$E_{SW}(OFF) = \int_o^{t_{fi}} V_{CE}\, i_c\, dt = \int_o^{2.5\times10^6} 8\times10^8\, t\left(1 - 4\times10^5\, t\right) dt$$

$$= 0.83\ \text{mJ}$$

$$\therefore\ E_{SW} = E_{SW}\ (ON) + E_{SW}\ (OFF) = 1.66\ \text{mJ}$$

$$\therefore\ P_{SW} = E_{SW} \times f_{SW} = 1.66\times10^{-3}\times 10 \times 10^3 = 16.6\ \text{watts.}$$

Conduction loss occurs in the interval from the end of t_{ri} to the beginning of t_{fi}

$$\therefore\ E_{COND} = V_{CE}\big|_{sat} \times I_L \times \left(T_{ON} - td - t_{ri} + t_s\right)$$

$$= 0.103\ \text{mJ}$$

$$\therefore\ P_{COND} = E_{COND} \times f_{SW} = 0.103 \times 10^{-3} \times 10 \times 10^3 = 1.03\ \text{watts.}$$

4. For the transistor Q, $\beta\big|_{Min} = 10$, & $i_c = 50$ A.

$\therefore$ required positive $i_{BP} = {}^{50}\!/_{10} = 5$ Amps

Now $i_{BP} = i_{E1} = i_{c1} + i_{B1}$

Now $i_{B1} = \dfrac{12 - V_{AB} - V_{BE}}{R_1} = \dfrac{10.55}{R_1}$

$$i_{C1} = \frac{15 - V_{CE}\big|_{sat} - V_{BE}}{R_{BP}} = \frac{14.1}{R_{BP}}$$

So $\dfrac{10.55}{R_1} + \dfrac{14.1}{R_{BP}} = 5$

Now $i_{BN} \geq i_{BP} = 5$A

$$i_{BN} = i_{E2} = i_{B2} + i_{C2}$$

$$i_{B2} = \frac{V_{BE} - V_{BA} + 12}{R_1} = \frac{12.05}{R_1}$$

$$i_{C2} = \frac{V_{BE} - V_{EC2} + 15}{R_{BN}} = \frac{15.55}{R_{BN}}$$

So $\dfrac{12.05}{R_1} + \dfrac{15.55}{R_{BN}} \geq 5$

Now β_{min} of Q_P & Q_N are same.

$$\text{So } \frac{i_{C1}}{i_{B1}} = \frac{i_{C2}}{i_{B2}}$$

$$\text{or } \frac{14.1}{10.55}\ \frac{R_1}{R_{BP}} = \frac{15.55}{12.05}\ \frac{R_1}{R_{BN}}$$

$$\text{Now } 1 + \frac{14.1}{10.55}\ \frac{R_1}{R_{BP}} = \frac{5R_1}{10.55}$$

$$1 + \frac{10.55}{12.05}\ \frac{R_1}{R_{BN}} \geq \frac{5R_1}{12.05}$$

$$\therefore\ 0 \geq 5R_1\left(\frac{1}{12.05} - \frac{1}{10.55}\right)$$

$$\text{or } R_1 > 0$$

$$\text{choose } R_1 = 100\,\Omega$$

$$\therefore\ R_{BP} = 2.88\,\Omega$$

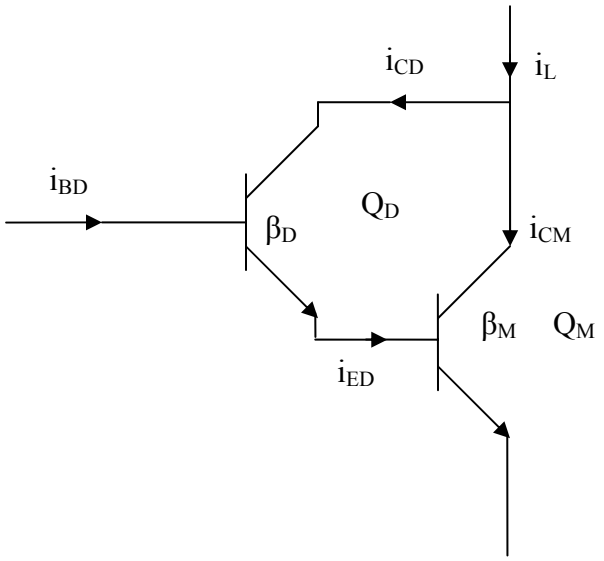
$$R_{BN} = 2.78\,\Omega$$

5. The main reason for comparatively lower dc current gain in a power transistor is a relatively thicker base region (a few tens of μm compared to a fraction of a μm incase of a signal transistor). The thicker base region is required to withstand the large blocking voltage. Unlike a power diode the doping density of the base region cannot be made very much large compared to the lightly doped collector drift region since it will reduce "β" by increasing minority carrier injection into the emitter. As a result the depletion layer at the C-B junction penetrates considerably in to the base region. The base width has to be larger than this penetration depth. A thicker base leads to larger rate of recombination of minority carriers injected by the emitter. Therefore, for a given collector current the required base current is relatively high and the dc current gain is low.

   A second reason for lowering of β arises from the "emitter crowding" effect where by the collector current tends to "crowd" near specific regions of the emitter. In these localized high current density regions β tends to fall off very sharply reducing the effective dc current gain.

   Due to lower dc current gain the base current requirement of a power transistor switching circuit increases. This requires a large base drive power supply and increased base drive power loss.

   This problem can be solved to some extent by using two power transistors connected in the "Darlington configuration" as shown.



For this configuration.

$$i_L = i_{CD} + i_{CM}$$

$$\text{But } i_{CD} = \beta_D\, i_{BD}$$

$$i_{CM} = \beta_M\, i_{ED} = \beta_M\,(i_{BD} + i_{CD})$$

$$\therefore i_L = \beta_D i_{BD} + \beta_M i_{BD} + \beta_M \beta_D i_{BD}$$

$$= (\beta_M + \beta_D + \beta_M \beta_D)\, i_{BD} = \beta_{eqv}\, i_{BD}$$

equivalent β (β_{eqv}) can be increased considerably due to multiplication of β_M & β_D.

Power Darlington has one problem, however. The main transistor (Q_M) does not go into hard saturation due to V_{CE} drop of Q_D. Therefore, the conduction loss is higher.

6. The voltage rating V_{SUS} is the maximum allowable voltage across C & E when the transistor is in active region with $i_B > 0$ and collector current above a minimum value.
With both i_B and i_C greater than zero, there is considerable supply of minority carriers which are accelerated by the large CB junction electric field to start avalanche breakdown at a relatively lower voltage. Therefore, the voltage rating V_{SUS} is the lowest of the three.

   The rating V_{CEO} is the maximum allowable voltage between C & E terminals when the transistor is in cut off region with $i_B = 0$ or i_C is less than a specified value. Under this condition the supply of minority carriers at the CB junction is much less compared to the previous case. Therefore, avalanche breakdown of the CB junction occurs at a higher voltage. Thus $V_{CEO} > V_{SUS}$.

   The rating V_{CBO} is the maximum allowable voltage between C & E terminals when the transistor is in cut off with $i_B < 0$ and i_C less than a specified value. With $i_B = 0$ the EB junction is still forward biased and there is small injection of minority carriers from the emitter to the CB junction. However, with $i_B < 0$ base emitter junction is reverse biased and there is no supply of minority carriers to the CB junction from the emitter. Thus avalanche

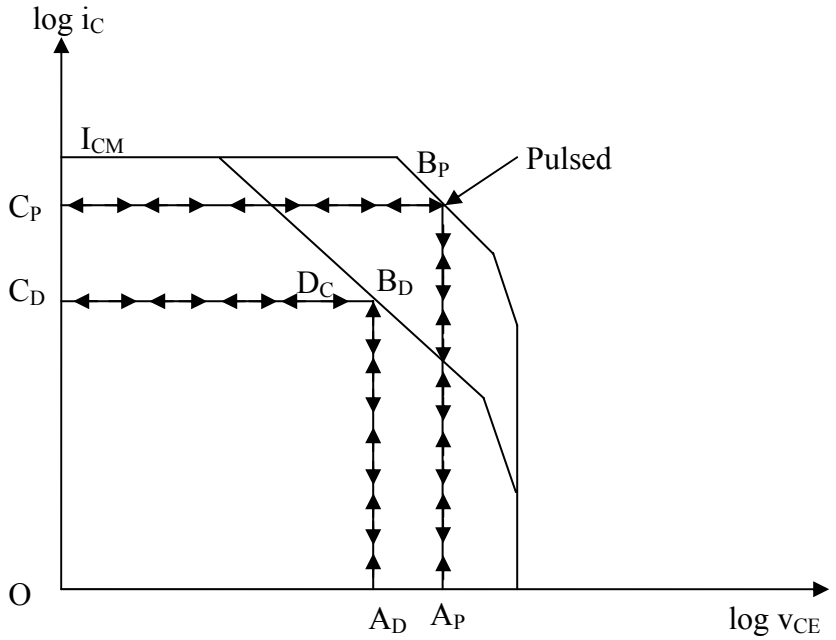
break down of this junction occurs at a relatively higher voltage making the rating V_{CBO} largest of the three. Therefore, in general for a power transistor.

$$V_{CBO} > V_{CEO} > V_{SUS}$$

In an inductive switching circuit using snubber the collector voltage falls considerably before i_C builds up to any significant level. This can be utilized to increase the usable steady state blocking voltage of the transistor up to V_{CEO}. Since V_{CE} will go below V_{SUS} before i_C can build up to the level where the rating V_{SUS} becomes applicable.

Similarly during turn off, the overshoot in the V_{CE} voltage can be accommodated in the difference between V_{CBO} and V_{CEO}. Since during turn off $i_B < 0$ and the voltage. overshoot occurs with $i_C = 0$ the applicable voltage limit will be V_{CBO} and not V_{CEO}. However, precaution must be taken such that the voltage over shoot decays before i_B becomes equal to zero.

However, if a snubber circuit is not used the applicable voltage limit will always be V_{SUS} since in this case V_{CE} does not fall till i_C rises to its full value during turn ON. Similarly during turn off i_C does not fall till V_{CE} rises to steady state blocking voltage level.



7. The main difference between the DC and pulsed FBOSA is in the boundary corresponding to maximum power dissipation and second break down. With only DC FBSOA the switching trajectory has to be restricted to something similar to A_D B_D C_D. However, with pulsed FBSOA applicable limits of power dissipation and second break down increases considerably. Both these limits require simultaneous existence of nonzero V_{CE} & i_C which for a power transistor occurs only during switching. Therefore, the increases FBSOA can be utilized and the switching trajectory improved to A_P B_P C_P provided total switching time is less than the pulse period for which the increased FBSOA is applicable.

In addition pulsed FBSOA s are usually specified for a very low duty ratio. This condition can be easily satisfied provided total turn on and turn off times of the transistor expressed as a percentage of total “ON” and “OFF” periods of the transistor is less than this duty ratio since during ON or OFF period the transistor remain well within DC FBSOA. In practice this condition is satisfied by specifying a minimum ON and OFF period of the transistor.